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Substrate Resistance Effect on Charge Pumping Current in Polycrystalline Silicon Thin Film Transistors

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1. Introduction

In polycrystalline silicon thin film transistors (poly-Si TFT's), there are many traps both in the grain and at the grain-boundary, which greatly influence electrical characteristics of the devices. Therefore, it is important to evaluate the trap properties. It has been known that the density and energy distribution of the traps can be determined from the capacitance and admittance measurement of a metal-oxide-semiconductor structure [1],[2] or the conductivity measurement [2],[3]. The drawback of these methods is that they cannot be applied directly to real devices. The charge pumping method (CPM) has been used to evaluate the grain-boundary trap properties of poly-Si TFT's [4],[5], which was originally developed for c-Si MOSFET's. In applying CPM to poly-Si TFT's, however, we should consider anomalous charge pumping current (I_{cp}). In this paper, we present a model for I_{cp} of poly-Si TFT's, which includes effects of large substrate resistance. The model could explain the anomalous I_{cp}, which is conformed the model by experiments.

2. Model Establishment

Experimental configuration is illustrated in Fig. 1 with a pulse shape. We measured I_{cp} of n-channel TFT by keeping the high level of pulse (V_h) constant with varying the base level (V_b). Figure 2 shows typical I_{cp} of both poly-Si TFT's and c-Si MOSFET's as a function of V_b. In c-Si MOSFET's, the current is saturated when the pulse amplitude is large enough to accumulate the surface. In poly-Si TFT's, however, the current keeps on increasing as the pulse amplitude increases. This phenomenon can be explained by a geometric component like in c-Si MOSFET's [6]. In c-Si MOSFET's, this geometric component is suppressed by forcing reverse voltage, V_r, to the source and drain and using gate pulses whose rising time, T_R and falling time, T_F are larger than 10nsec for devices with W/L>1. In poly-Si TFT, however, I_{cp} does not saturate although all the conditions are satisfied. Fig. 3 is the measurement results of substrate current by varying the gate pulse frequency. I_{cp} increases as the gate pulse frequency increases in c-Si MOSFET as expected in the conventional theory. In poly-Si TFT, however, I_{cp} even decreases.

To explain these phenomena, we considered the large substrate resistance of poly-Si and suggested a device model with distributed resistance and capacitance. The model is simplified by using lumped parameters, R_{eq} ($R_{eq,e}$ for electrons and $R_{eq,h}$ for holes) and C_{ox}, as shown in Fig. 4. R_{eq} is calculated by the sheet resistance and device geometry and C_{ox} by the gate oxide thickness and area. Then, the amount of remained electron, $Q_e(t)$, when the gate voltage changes from V_h to V_b (for t>0 in Fig.1), is

$$Q_e(t) = C_{ox}\left|V_h - V_{TH}\right| exp\left(-\frac{t+T_{o,e}}{R_{eq,e}C_{ox}}\right) - Q_{rec}(t)$$

where $T_{o,e} = \frac{\left|V_{TH}-V_{FB}\right|}{\left|V_h - V_b\right|} T_F$. The amount of supplied holes is

$$Q_h(t) = C_{ox}\left|V_b - V_{FB}\right| exp\left(-\frac{t}{R_{eq,h}C_{ox}}\right) - Q_{rec}(t)$$

$Q_{rec}(t)$ is the amount of free charges, which recombine under the gate and given by

$$Q_{rec}(t) = \alpha \cdot Q_e(t) \quad \text{if} \quad Q_h(t) > Q_e(t)$$
$$Q_{rec}(t) = \beta \cdot Q_h(t) \quad \text{if} \quad Q_h(t) < Q_e(t)$$

where α and β are constant. The current by recombination of free carriers, which is called geometric component, is calculated by differentiating $Q_{rec}(t)$ by time. By numerical analysis, we calculated the geometric current with varying T_R and T_F, which is illustrated in Fig. 5. The geometry component is dependent on T_R and T_F. In poly-Si TFT's, therefore, it is not reliable to extract the energy distribution of traps from T_R and T_F dependence of I_{cp}.

Another problem caused by the large substrate resistance is that the carrier supply is suppressed especially at a high frequency range. We modeled this phenomenon and the simulation results are also plotted in Fig. 5 for a device with the trap density of $2.6\times10^{11}cm^{-2}$ [7]. Total current coincides well with the measured I_{cp}.

3. Experimental Results

To analyze the trap properties, n-channel poly-Si TFT's were fabricated with three different kinds of gate oxide. One group has a 9.7nm-thick thermal oxide grown at 900°C in dry O_2. The second has a 13.1nm electron cyclotron resonance (ECR) O_2-plasma oxide. The third has a 12nm-thick ECR N_2O-plasma oxide. The trap densities evaluated by the model (*freq*=1kHz and T_R and T_F are 200μsec) are $12.19\times10^{12}cm^{-2}$ for thermal, 6.86×10^{12} cm^{-2} for ECR O_2, and 3.54×10^{12} cm^{-2} for ECR N_2O oxide. The lower trap density, the superior electrical characteristics of the devices are (I_{DS}-V_{GS} of poly-Si TFT's are shown in Fig. 6). More study on the relation of trap and electrical characteristics is performed by using the suggested charge pumping model.

4. Conclusion

In applying CPM to poly-Si TFT's, the large substrate resistance slows the carrier transit and reduces the carrier supply especially at a high frequency range. The former increases the geometric component. Therefore, we should use gate pulses whose T_R and T_F are sufficiently long to cut out the geometric component. It means that we should choose gate pulses carefully when we extract the energy distribution of traps from the T_R and T_F dependence of I_{cp}. The latter suppresses I_{cp} by limiting carrier supply. We suggest a model which explains well the measured I_{cp} of poly-Si TFT's. From the model, we could find proper conditions for I_{cp} measurement and we evaluated trap properties of three different kinds of poly-Si TFT's.

References

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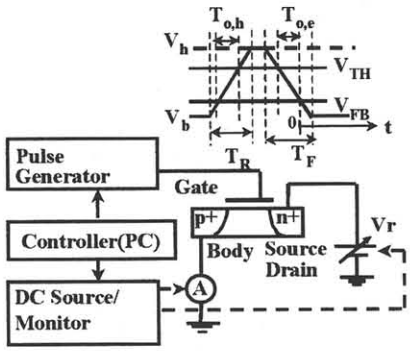

Fig. 1 Experimental configuration and gate pulse shape.

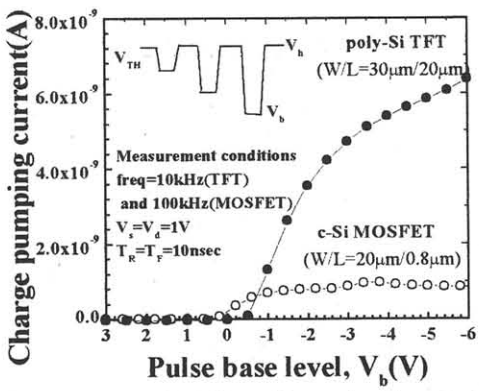

Fig. 2 Measurement results of I_{cp} with varying the pulse base level while keeping the high level constant. For comparison, I_{cp} of c-Si MOSFET are measured.

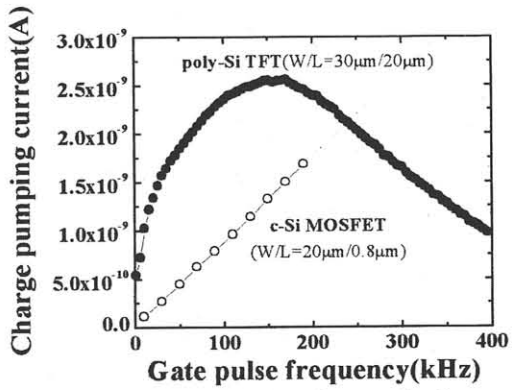

Fig. 3 Measured I_{cp} as a function of gate pulse frequency. T_R and T_F are four tenth of pulse width (Here, pulse width is T/2 when the pulse period is T).

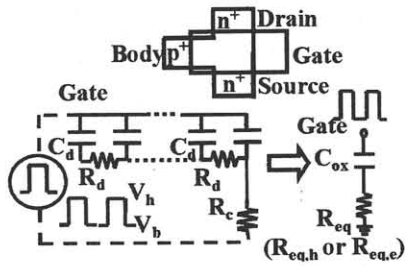

Fig. 4 A suggested model of poly-Si TFT's for the charge pumping current.

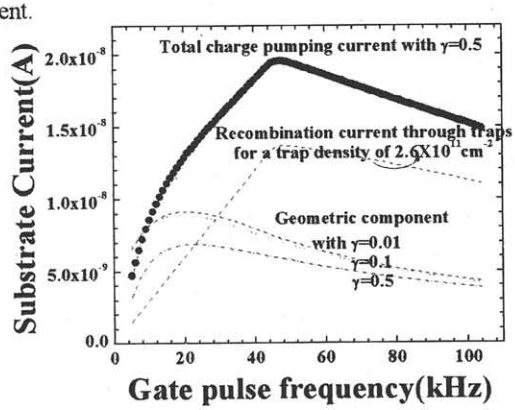

Fig. 5 Geometric components calculated by the suggested model for a device of which C_{ox} is 0.81pF and $R_{eq,e}$ is 8.43Mohm and $R_{eq,h}$ is 83.43Mohm. α and β are assumed to be 1. γ is the ratio T_R and T_F to pulse width. The current by recombination through traps is simulated by considering the limited supply of carriers at a high frequency range.

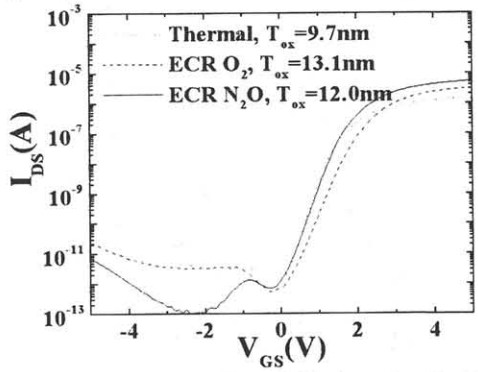

Fig. 6 Electrical characteristics of fabricated poly-Si TFT's at V_{DS}=0.1V. Device size (W/L) is 50μm/10μm..