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# 20V Operation Power GaAs MESFET with a Field-Modulating Plate

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## 1. Introduction

The new-era wireless-telecommunication-system, IMT-2000, requires much higher-power solid-state-amplifier for use in cellular base station. An increase in the operating voltage is a best solution for the purpose but several restrictions are often encountered such as a serious trade-off between the breakdown voltage and the RF power performance, e.g. output power and efficiency. The poor RF performance for the conventional GaAs FETs designed for high breakdown voltage is attributed to the surface trap effect[1-4], for which slow response of the charge/discharge of the trap near the gate freezes the channel modulation at RF. As a result, the operating voltage of GaAs power FETs has been usually limited within 10V.

The field plate has been proposed to improve breakdown voltage[5] and has been commonly used in Si high voltage devices. A few studies have been reported for GaAs FETs to improve breakdown voltage. In addition to this feature, we noticed that a field plate has a capability of modulating the channel opening at RF even if the response of surface trap is quite slow. Hence we expect, if the surface depletion layer is modulated along with the gate voltage, much higher operating voltage without degrading the RF power performance for GaAs-based FETs.

In this work, we have developed a novel high power GaAs FET tagged with a field-modulating plate (FPFET) which accomplished both improvement of the gate-drain breakdown voltage above 40V and excellent RF power performance which is further evidenced by drastic suppression of the drain-current-pulse dispersion. The much superior RF operation at over 20V drain voltage is also demonstrated.

## 2. Device structure and fabrication

The schematic cross-sectional view of the fabricated FPFET is shown in Fig.1. A field-modulating plate was formed on the $SiO_2$ surface passivation layer in the gate-drain recessed region of the conventional MESFET structure. The epitaxial layers consist of a buffer layer, an n-type GaAs active layer doped with Si of $2 \times 10^{17}$ $cm^{-3}$ and an n+ contact layer. The gate electrode was formed in the recessed region by using the WSi/Au gate metalization process. After the deposition of $SiO_2$ passivation layer (100nm thick), a field-modulating plate of Ti/Au was formed by using conventional lift-off process. Gate electrode and field-modulating plate were connected at the gate feed by the through-hole and air-bridge formation, and hence the both electrodes are modulated in phase with the input signal. The gate length is 1μm and the recess length between gate and recess edge at the drain side, shown as Lgdr in Fig.1, is 2.5μm.

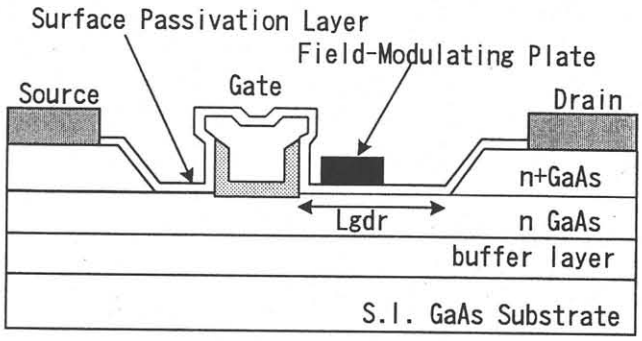
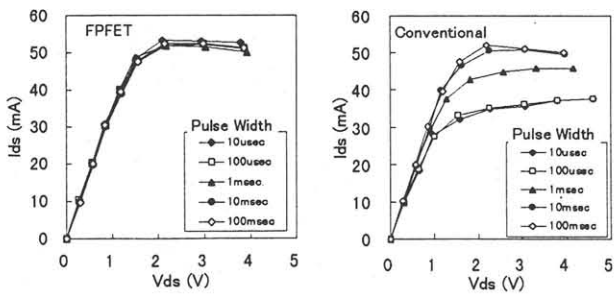



Fig.1 Schematic cross-sectional view of the FPFET

## 3. Device performance

The fabricated GaAs FPFET exhibited a gate-drain breakdown voltage of about 40V, which is 30 ~40% higher than that of the conventional FET. This improvement is attributed to the reduction of the electric field near the gate edge by introducing the field-modulating plate. Other DC characteristics, such as the threshold voltage Vt or the saturation drain current Idss were almost the same as those of the conventional FET, where Vt and Idss were about –2V and 200mA/mm, respectively.

For examining the effect of field-modulating plate under large signal operation, the pulse response of drain current was evaluated by using the test circuit described previously[4]. The gate was pulse-biased from –3V to +0.8V with the pulse width between 10μsec to 100msec and the drain current was measured while the FET was turned on. Figure 2 shows the pulsed I-V characteristics of the fabricated devices with a gate width of 200μm. Although a conventional FET exhibited serious reduction in the drain current as the pulse width was decreased from 100msec to 10μsec, the FPFET showed almost no change in the drain current. This drastic suppression in the drain current dispersion suggests that the field-modulating plate acts as a MIS gate and effectively controls the depletion layer in the gate-drain recessed region, resulting in the removal of channel constriction effect caused by




(a) FPFET (b) conventional

Fig.2 Pulsed I-V characteristics of (a)FPFET and (b) conventional FET.

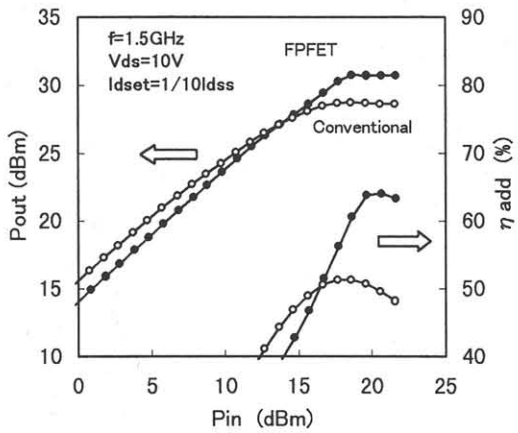



Fig.3 Pin versus Pout of fabricated devices at 10V.

surface traps under large signal operation.

Power performance was evaluated for devices with a gate width of 2.6mm at 1.5GHz. Figure 3 shows the input power versus output power relation of the fabricated device measured at a drain bias voltage of 10V and a drain bias current of 10% Idss(class AB). The FPFET showed good linearity and higher output power and power added efficiency than those of the conventional FET, suggesting that field-modulating plate effectively improves the channel constriction caused by the surface trapping effect in accordance with Fig.2. Linear gain of the FPFET was slightly lower than that of the

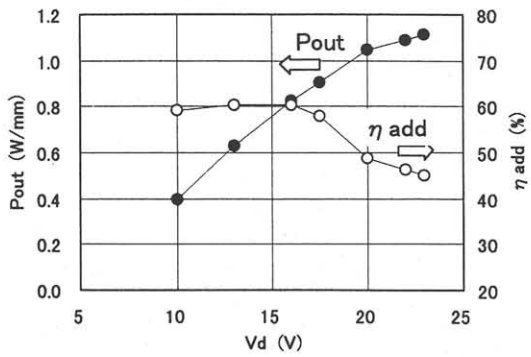



Fig.4 Drain voltage dependence of Pout and η add

conventional FET. This is attributed to higher feedback capacitance, which can be minimized by optimizing the field-modulating plate structural parameters. Figure 4 shows the drain voltage dependence of output power and power added efficiency. The FPFET showed a marked increase in the output power up to 20V and held high power added efficiency of more than 60% up to 16V. Figure 5 shows the power performance measured at Vd=23V, indicating maximum output power of 1.1 W/mm.

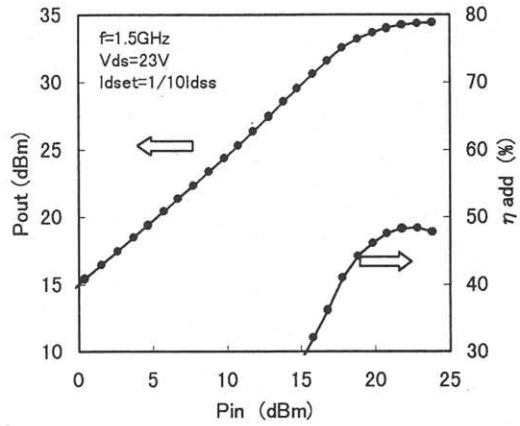



Fig.5 Pin versus Pout of FPFET at 23V.

## 4. Conclusion

We have developed a novel power GaAs MESFET with a field-modulating plate (FPFET), which accomplished both the improvement of the gate-drain breakdown voltages above 40V and the drastic suppression of the drain-current-pulse dispersion. The FPFET demonstrated excellent power performance at high drain voltages more than 20V. These results indicate that the FPFET is promising as a power device for high voltage operation.

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