Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 394-395

Analysis of Electric Field Distribution in Novel GaAs MESFET with a Field-Modulating Plate

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1. Introduction

Significant improvements both in the breakdown voltage and the microwave power performance were demonstrated by employing a novel GaAs MESFET with a field-modulating plate (FPFET), where the field-modulating plate (FP), whose potential is kept equal to that of the Schottky gate, is placed between the gate and the drain recess edge [1]. The FPFET is thus structurally different from the conventionally proposed overlapping-gate FET [2,3]. The effects of structural FPFET parameters, such as the FP length (L_F) and the distance between FP and the gate (L_{GF}), on the breakdown behavior have not yet been studied theoretically. In this paper, we report the potential distribution of the FPFET calculated using a 2D ensemble Monte Carlo simulation. The electric field in the channel of various FPFETs including that of the overlapping-gate FET will be discussed. Finally, experimental results of electro-luminescence intensity measurements performed on the surface of FPFET will be presented with reasonable agreements with the calculated field distribution.

2. Device Structure and Simulation Procedure

The FET structure employed for the theoretical analysis is a recessed-gate GaAs MESFET with a gate length of 0.9μm and a gate-drain recess distance of 2.5μm. The doping density of the n-type GaAs channel layer was chosen to be $2 \times 10^{17}cm^{-3}$. We assumed a dielectric film of 0.1μm thick SiO_2 deposited on the recess surface of the channel layer and the FP electrode placed on the SiO_2 film between the gate and the drain-side of the recess edge (see Fig. 1).

To precisely take account of the high-field electron transport phenomenon, we have employed an ensemble Monte Carlo model incorporating a nonparabolic Γ-L-X analytical band for GaAs. The model includes polar optical phonon scattering, intervalley deformation potential scattering, and ionized-impurity scattering. During the simulation, no bulk charge was assumed within the SiO_2 film and the FP voltage (V_{FP}) was kept equal to the gate voltage (Vgs).

3. Results and Discussion

Figure 1 shows calculated potential distributions for the conventional MESFET (with no FP electrode) and the FPFET. The devices were biased at Vds=20V and at Vgs=-0.8V, where drain current of about one half of Imax flows for both FETs. Note that an additional high-field region was produced under the FP electrode for the FPFET.

Figure 2 plots the electric field distribution along the channel. It is obvious that the introduction of the FP electrode contributes to the relaxation of electric field at the drain-side of the gate edge.

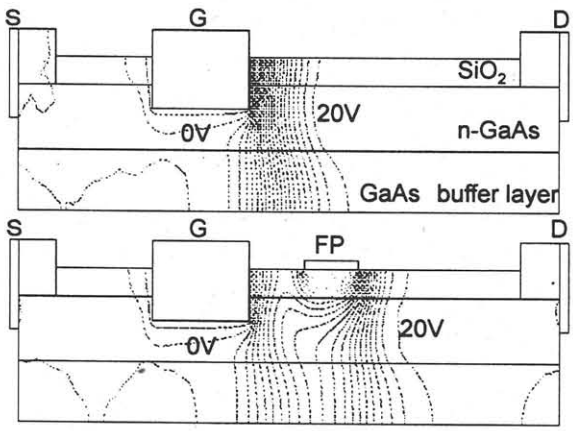

Fig. 1. Potential distributions for conventional MESFET (upper) and FPFET (lower) biased at Vds=20V and at Vgs(=V_{FP})=-0.8V.

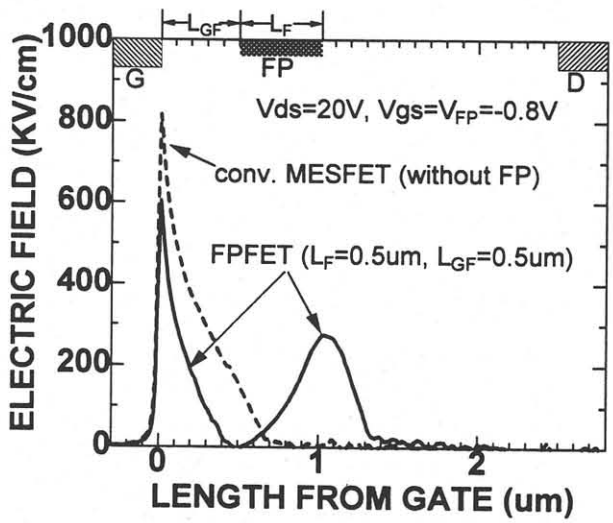

Fig. 2. Electric field distributions in the channel for conventional MESFET and FPFET biased at Vds=20V and at Vgs(=V_{FP})=-0.8V.

Figure 3 shows the peak electric field at the gate edge as a function of the position of the FP electrode (L_{GF}). The peak electric field at the FP edge is also plotted in Fig. 3. It was found that the field intensity at the FP edge does not exceed that at the gate edge and is relatively insensitive with respect to the changes in both L_{GF} and L_F. On the other hand, the peak electric field at the gate edge exhibited significant dependence on L_{GF} and L_F, where we noticed a general trend that the field intensity reduces with the decrease in L_{GF}. However, an exceptional behavior was seen for the FPFET with a small L_F value, i.e., typically less than 0.5μm, where the electric field at the gate edge for L_{GF}=0μm (corresponding to the overlapping-gate FET) is larger than that for the FPFET with a finite value of L_{GF} (<0.5μm). This indicates that the vertical field termination at the FP electrode for the FPFET becomes more efficient than the overlapping-gate FET, leading to a more reduced electric field for the FPFET, when L_{GF} is smaller than the high-field region length near the gate edge, which is typically about 0.5μm. These results suggest that the FPFET structure can be optimized simultaneously for high breakdown voltage and for high-frequency operation when a reduced size of FP is adopted.

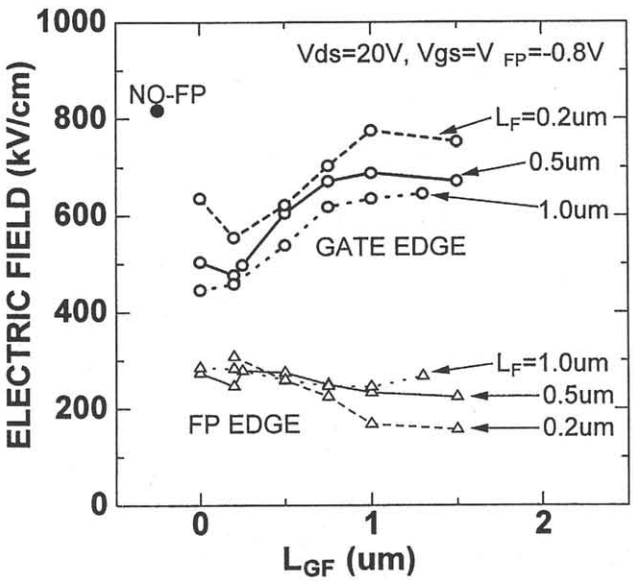

Fig. 3. Peak Electric field at gate and FP edges as a function of L_{GF} for FPFETs (L_F=0.2, 0.5, 1.0μm) biased at Vds=20V. Peak electric field at the gate for MESFET (NO-FP) is also shown.

In order to verify the field distribution in FET experimentally, we have measured the spatial intensity distribution of electroluminescence (EL) emitted from the surface of the FPFET under high-voltage operation (Vds=20V). As shown in Fig. 4, we can see two strong EL peaks, i.e., one at the gate edge and the other at the FP edge. The positions of these two peaks correspond to those for the calculated electric field peaks, as already shown in Figs. 1 and 2. These results suggest the validity of the FET model employed in this simulation.

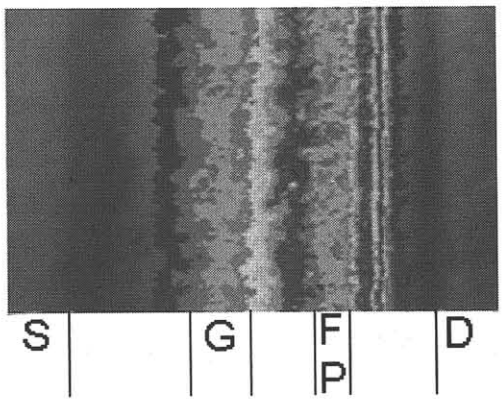

Fig. 4. Spatial distribution of electroluminescence from FPFET biased at Vds=20V and at Vgs=-0.1V.

4. Conclusion

The electric field distribution in the channel of FPFET has been theoretically investigated. The electric field intensity at the gate edge was significantly relaxed by the introduction of the FP electrode. From the field intensity calculated as a function of L_F and L_{GF}, the peak electric field for FPFET with a finite value of L_{GF}<0.5μm has been found to be reduced compared to that for the overlapping-gate FET when a small L_F (<0.5μm) is preferred. These results indicate that the optimized FPFET with smaller L_{GF} than the high-field region length near the gate edge is especially promising as a high breakdown voltage device for higher-frequency operations.

Acknowledgement

The authors would like to thank K. Asano, N. Iwata, Y. Ando, W. Contrata, Y. Mochizuki and Y. Ohno for their fruitful discussions. They also thank M. Ogawa, O. Mizuno, A. Higashisaka, T. Uji, K. Ueda and N. Samoto for their encouragement throughout this work.

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