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High Current/gm Self-Aligned PJ-HFET of Completely Enhancement-Mode Operation

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1. Introduction

For cellular phones, power amplifiers are required to operate at low voltages with high efficiencies. The Id-Vgs curves for three different types of HFETs are shown in Figure 1. Although power amplifiers using depletion-mode Schottky Gate HFETs (SG-HFET) have high drain current characteristics and high efficiencies, they require two voltage supplies both negative and positive for operation. For the single supply voltage operation, slightly depletion-mode SG-HFETs have been employed so far[1-2]. These depletion-mode SG-HFETs, however, require drain switch because their drain currents in the standby mode are too high. Therefore, completely enhancement-mode SG-HFETs are strongly demanded to eliminate the extra circuit for the negative voltage supply and also a drain switch. The problem for the completely enhancement-mode SG-HFETs is that a large forward gate voltage (Vgs) swing cannot be realized because of their low built-in voltage.

In this work, we report the first successful fabrication of self-aligned P+-GaAs Junction HFETs (PJ-HFETs) of completely enhancement-mode operation capable of a larger Vgs swing more than 1.5V by exploiting the higher built-in voltage of p/n junctions.

2. Device and Processing

A schematic cross-section of the epitaxial structure of the ion-implanted self-aligned PJ-HFET is shown in Figure 2. The structure consists of pseudomorphic double heterojunction N-AlGaAs/InGaAs/N-AlGaAs layers and top p+-GaAs layer. The doping level of the p+-GaAs layer was 2.0×10^{19} cm^{-3}. The AlAs mole fraction in the AlGaAs layers was 0.25 and the doping level of Si in the N-AlGaAs layers was 2.0×10^{18} cm^{-3}.The In mole fraction in the InGaAs layer was 0.2. The WSi metal was formed by DC sputtering and reactive ion etching. The unnecessary p+-GaAs layer was etched off using WSi as a mask. The n+ regions self-aligned to WSi were formed by Si ion implantation into the epitaxial layers. Si implantation was performed at an energy of 30 keV with a dose of 5×10^{13} cm^{-2}. In order to obtain high activation for Si implanted layers without degrading the characteristics of the unimplanted regions, we adopted hot-plate annealing using a graphite heater and the annealing was performed at 750 ℃ for 30 seconds in a hydrogen atmosphere with a SiO_2 capping film. This condition was suitable for minimizing both the sheet resistance of the implanted layer and the WSi/p+-GaAs contact resistance. Following the high temperature anneal, the devices were isolated by boron implantation. Ohmic contacts were formed by evaporation of AuGe/Ni/Au. Finally, Ti/Au was deposited as a gate over-layer to reduce the overall gate resistance and interconnect metal.

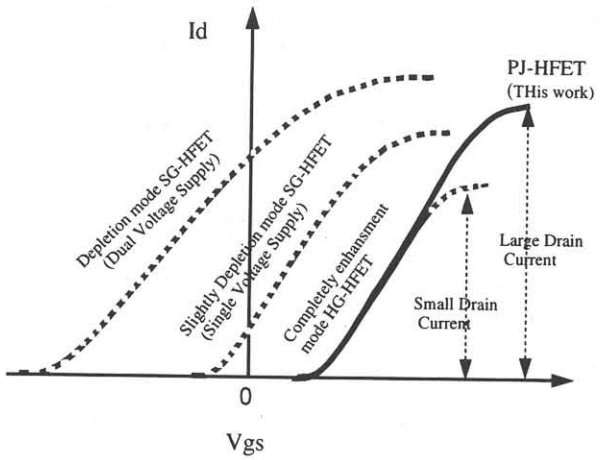

Fig. 1 Id-Vgs curves for three different types of HFETs

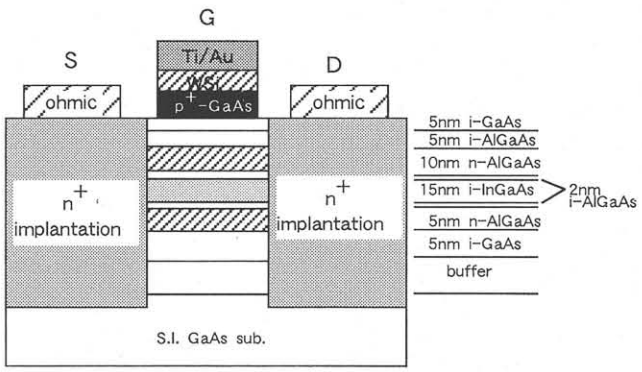

Fig. 2 Cross sectional view of the self-aligned PJ-HFET

3. Characteristics

From the measured diode forward I-V characteristics for the J-HFET and the WSi-gate SG-HFET, the barrier height was 1.12 eV for PJ-HFETs and 0.81 eV for SG-HFETs. The ideal factor was almost same (1.14) for both devices. Because of p/n junction, the barrier height of PJ-HFETs was higher than that of SG-HFETs by about 0.3 eV.

Figure 3 shows the typical Ids, gm-Vgs characteristics of a 0.8μm-gate PJ-HFET with 100μm gate width compared with 0.8μm-gate WSi-gate SG-HFET which has same threshold

voltage (Vth) as that of the PJ-HFET.

Vth of these HFETs determined by linear extrapolation of the square root of the drain current were about 0.2 V at Vds of 3 V. A high maximum drain current (I_{MAX}) of 380 mA/mm at Vgs of 1.5 V was obtained in the PJ-HFET because of large voltage swing. On the other hand, the I_{MAX} of the SG-HFET was 300mA/mm at Vgs of 1.0 V. The PJ-HFET exhibited a high maximum transconductance (gm_{MAX}) of 410 mS/mm at Vgs of 1.35 V as compared with that of the SG-HFET of 340 mS/mm at Vgs of 1.0 V due to the high barrier height of p/n junctions. The K-value of PJ-HFETs was 400 mS/Vmm and the drain-source leakage current was as low as 0.5 μA/mm at Vgs=0V. The source resistance was 2.6 Ωmm and the sheet resistance of n^+ layer was 500 Ω/□. The typical gate-drain breakdown voltage was -10 V measured at a gate-drain current of 100 μA/mm. The Vth values for 35 devices across a 3 inch wafer were measured to confirm the uniformity of the device characteristics. The average Vth of 0.19 V and a standard deviation of 18.4 mV have been obtained.

Figure 4 shows input-output power performance of the PJ-HFET (Wg=3.2mm) together with the characteristics of adjacent channel leakage power ratio(ACPR), operation current(Id) and power added efficiency(PAE). Very low operating current of 99mA was achieved at Pout=21.5dBm with high PAE of 39.5% and low ACPR of -57.4 dBc operated with a single drain bias of 3.3V. Here, the idle current was 55mA and ACPR is measured at 600 kHz off center frequency of 1.9 GHz. The characteristics of this PJ-HFET satisfies the requirements for low current operation in the single voltage supply condition.

In the WSi-gate SG-HFET, Pout=21.5dBm was obtained for the device with larger gate width of 4mm and at higher operating current of 150mA with PAE of 28.0% and ACPR of -56.4 dBc. These results show the superiority of PJ-HFETs over SG-HFETs which resulted from the larger gate voltage swing in PJ-HFETs.

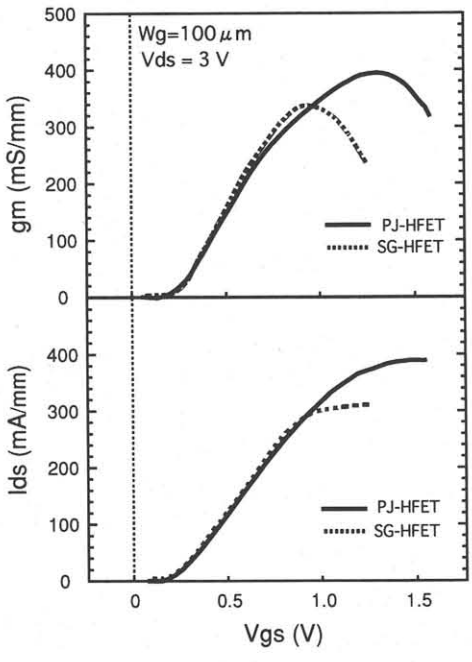

Fig. 3 Comparison of Ids, gm vs Vgs characteristics of PJ-HFET and SG-HFET

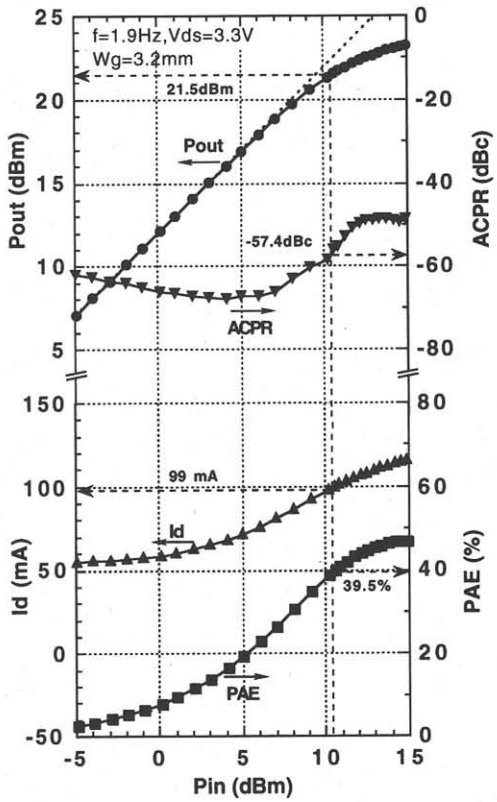

Fig. 4 Input-output characteristics with ACPR , Id and PAE of the PJ-HFET (Wg=3.2mm),
Input Signal : π/4 shift QPSK (PHS mode)

4. Conclusion

We have developed high current and gm self-aligned PJ-HFETs of completely enhancement mode operation. By utilizing the merit of p/n junction, the barrier height of 1.12 eV has been obtained. The 0.8 μm-gate PJ-HFET exhibited K-value of 400 mS/Vmm, gm_{MAX} of 410 mS/mm and I_{MAX} of 380 mA/mm with Vth of 0.2 V. Operated with drain bias of 3.3 V, the PJ-HFET demonstrated PAE of 39.5% with ACPR of -57.4 dBc at Pout =21.5 dBm and f=1.9 GHz. These excellent results suggest that the PJ-HFETs and its process are very suitable for the fabrication of GaAs power MMIC's operated with a single voltage supply.

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