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Annealing Behavior of Low-Temperature-Deposited $SrTiO_3$ Capacitor

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1. Introduction

In recent years, low-temperature-deposited-$SrTiO_3$ (LTD-STO) capacitor has been extensively applied for the bypass-capacitor of GaAs-MMIC[1),2)3)]. In order to use this capacitor in matching circuits, the capacitance deviation should be within ±5%. Therefore, the uniformity and reproducibility of the dielectric constant (ε_r) is required for LTD-STO.

However, the εr of the LTD-STO varies due to the processing steps following the capacitor formation. Figure 1 shows the dependence of the εr distribution across a 3 inch wafer vs 450℃ annealing time. This temperature is the same as the ohmic alloying temperature of GaAs-FET. The ε_r was widely distributed after the annealing, and the average capacitance was also increased. However, the εr distribution was decreased by increasing the annealing time. In order to obtain the accurate capacitance, it is important to investigate this ε_r variation phenomena. In this paper, we studied the thermal behavior of the LTD-STO capacitor, and investigated the relationship between the dielectric properties and the relaxation of the distortion in the STO film. We will be able to control this relaxation by adopting the annealing process subsequently after the STO deposition.

2. Experiments

The STO films were deposited by RF magnetron sputtering over Pt bottom electrode prepared on a SiN/GaAs substrate. The deposition temperature was 300℃, and film thickness was 300nm. After WSiN top electrode deposition, Ar ion milling was employed to pattern the STO capacitor. The fabricated capacitor area was $100\times100\,\mu m^2$. The εr was measured at a frequency of 1MHz using a C-V meter. XRD measurement was used to characterize the crystallinity of the STO films.

3. Results and Discussion

We compared the STO charateristics with as-deposited STO (Sample A) and after the 450℃ 30min annealed sample (Sample B) as shown in Fig. 1. Figure 2 shows the dependence of the capacitance on bias voltage for these two samples. The measurement was carried out both with increasing and decreasing the bias voltage. Small hysterisis can be seen in Sample A. This result suggests the as-deposited film may have a ferroelectricity caused by the crystal distortion in the STO crystal structure. On the contrary, no hysterisis was observed in Sample B.

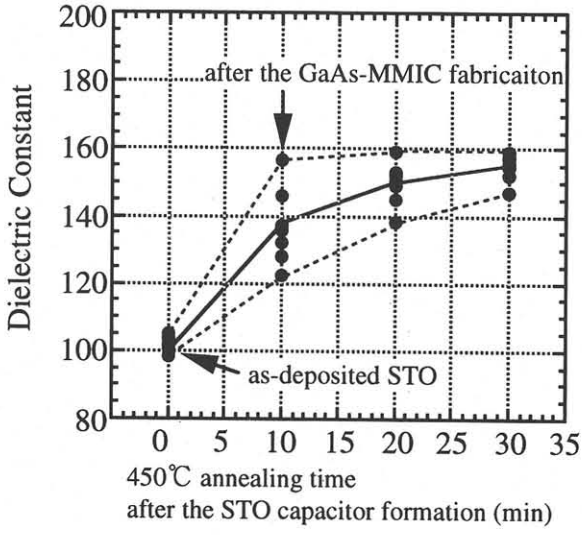

Figure 1: Dependence of the ε_r distribution across a 3 inch wafer on 450℃ annealing time.

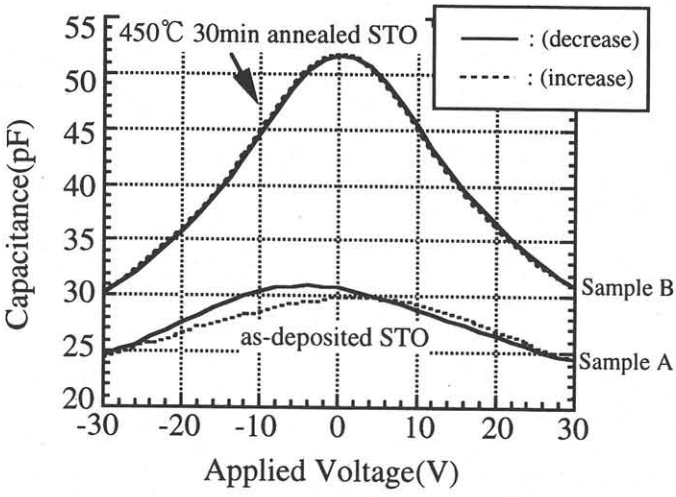

Figure 2: Dependence of the capacitance on bias voltage

X-ray diffraction measurements were carried out to evaluate this crystal distortion. Figure 3 shows the XRD pattern of these two samples after removing the upper electrode. Enhanced peak intensities were observed with Sample B compared with Sample A for each (100), (110), (2 11) direction. Moreover, the (110) peak shifted to a higher angle by the annealing(d=2.792 Å→2.769 Å). This value is close to the bulk STO crystal as shown in JCPDS (d=2.759 Å) after the annealing. These results suggest that this crystal distortion can be relaxed by the annealing. The variation of the capacitance is thought to be caused by this relaxation.

Therefore, the crystal distortion should be fully relaxed across the wafer to obtain stable and uniform capacitor characteristics. We studied effective relaxation method to obtain uniform crystallinity across the wafer. We performed the annealing subsequently after the STO deposition in order to exclude the influence of the upper electrode for the relaxation. The annealing was performed at 450℃ for 15min in N_2 ambient.

We compared the thermal stability and uniformity of the subsequent annealed STO capacitor with the as-deposited STO. Thermally stable and uniform capacitors were realized by adopting the subsequent annealing. The deviation of the εr was within ±5% across a 3 inch wafer. The εr variation was also suppressed by the subsequent annealing. The C-V hysteresis was not observed in this sample. This result indicates the subsequent annealed STO capacitor has less high frequency loss application than the as-deposited one. The subsequent annealing process is thought to contribute to the shrinkage of the size and the yield improvement of the GaAs-MMICs.

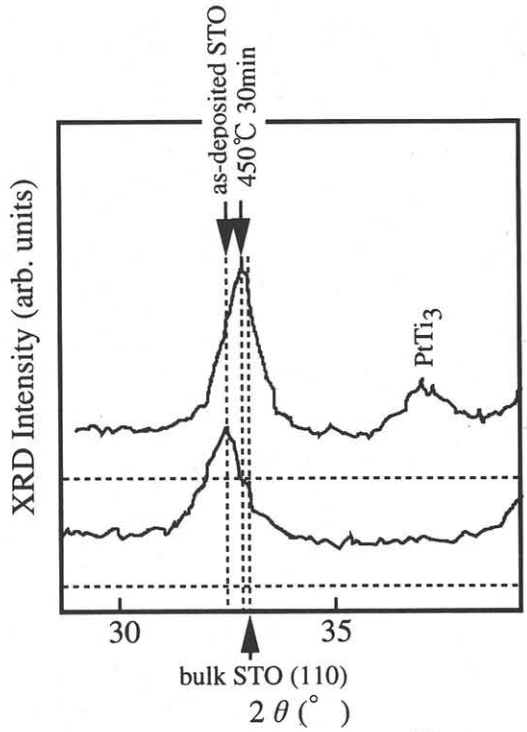

Figure 3: STO(110) peak shifts by the 450℃ 30min annealing

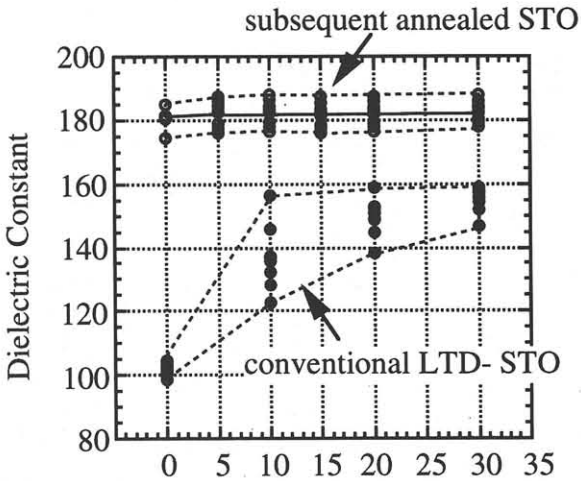

Figure 4: Thermal stability of STO capacitors

4. Conclusion

We applied the subsequent annealing for LTD-STO to obtain uniformity and thermal stability of the capacitor. The subsequent annealed STO film has no hysterisis, that is, no ferroelectricity in the film, and is thought to be highly suitable for high frequency application within GaAs-MMICs. These stable characteristics were caused by the relaxation of the crystal distortion introduced in as-deposited film.

Acknowledgments

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