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Simulation of the Influence of the Piezoelectric Effect on the Device Characteristics of AlGaN/GaN Insulated Gate Heterostructure FETs

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1. Introduction

We have previously proposed a novel AlGaN/GaN insulated-gate heterostructure Field Effect Transistor (FET) with modulation doping, and a simulation and experiments have shown the superiority of the structure [1][2]. In this AlGaN/GaN FET, a large piezoelectric effect (P.E.) is caused by a large lattice mismatch between the GaN (or AlGaN) substrate and the AlN (or AlGaN) layers [3]. In order to investigate the influence of this effect on the FET's characteristics, we simulated charge control including P.E., then compared the device characteristics of the FET with P.E. and without P.E.

2. Simulation Method

Charge control in the FET was simulated in one dimension by solving Poisson and Schrödinger equations self-consistently [1]. First, we calculated the charge distribution in the vertical structure of the FET, then the gate capacitances due to various charge components were calculated and finally the dependence of the transconductance G_m and the cut-off frequency f_T on the gate voltage were obtained. P.E. is taken into account in the simulation by solving the Poisson equation under the condition of continuity of the electric displacement including the electric polarization induced by P.E. at the heterointerface, namely $D_L(=\varepsilon_L E_L+P_L)=D_R(=\varepsilon_R E_R+P_R)$.

The three vertical structures of the FET used in the simulations are (1) AlN/GaN, (2) AlN(gate insulator)/GaN(channel)/$Al_{0.15}Ga_{0.85}N$(electron supply layer)/$Al_{0.4}Ga_{0.6}N$(barrier layer)/GaN (substrate) and (3) AlN/GaN/ $Al_{0.3}Ga_{0.7}N$ and are shown in Fig.1. We assume that all layers with wurtzite structure are grown in the direction of [0001] and each layer with a strain-unrelaxed lattice on the substrate has the same lattice constant as that of the substrate. Furthermore, the electric polarization of $Al_xGa_{1-x}N$ with a strain-unrelaxed lattice induced by P.E. is assumed to be $P(x)=3\times10^{-6}$ x Ccm^{-2} [4] and the Schottky barrier height between AlN and the gate metal is assumed to be 3.0 eV.

3. Simulation results

Figures 2 and 3 show G_m–V_{gs} characteristics and Figs. 4 and 5 show f_T–V_{gs} characteristics, for the three FET structures with and without P.E., respectively. By comparing these figures, we can see that P.E. shifts the threshold voltage of FET (V_{th}) in the three structures, ΔV_{th}= −1.5, −0.8, −1.0 V, respectively. Owing to this V_{th} shift, the effective gate voltage range widens by $|\Delta V_{th}|$. As a result, G_m and f_T with P.E. have wider flat regions than those without P.E. for all three structures. Moreover, G_m with P.E. has a higher value, while the value of f_T is almost the same in both cases. In both cases, the value of f_T slightly decreasing as V_{gs} increases in its high value region because of increasing two dimensional electron gas (2DEG) concentration penetrating into the gate insulator. Figures 2 and 4 compare G_m-V_{gs} and f_T-V_{gs} characteristics with P.E. among the three FET structures. Structure 1 has the widest gate voltage region with high G_m and f_T values. Structure 1 also has the maximum G_m value, higher than 3 S/mm.

The equilibrium 2DEG concentration without a gate metal is a very important figure of merit because it determines the parasitic resistance between gate and source/drain. We estimated the equilibrium channel carrier concentration (E.C.C.) with and without P.E. under the flat band condition for the three FET structures. E.C.C. with P.E. is 1.86×10^{13}, 1.47×10^{13} and 1.27×10^{13} cm^{-2} for structures 1, 2, and 3, respectively, while E.C.C. without P.E. is 0, 1.5×10^{12} and 0 cm^{-2}, respectively. Figure 6 shows 2DEG distribution in the device. In the case of structure 2, 2DEG is also induced in the substrate. The capacitive coupling of this 2DEG with drain/source may reduce the maximum oscillation frequency.

4. Conclusion

By comparing the simulation results with P.E. and without P.E., we found the following: (1) P.E. shifts the threshold voltage of FET (V_{th}) and widens the effective gate voltage range by $|\Delta V_{th}|$. (2) E.C.C. increases with the plus polarization charge due to P.E. This increased 2DEG concentration greatly reduces the parasitic resistance between the gate and the source/drain. (3) G_m–V_{gs}: With P.E., G_m is higher and the flat region is wider than without P.E. f_T–V_{gs}: The value of f_T is nearly the same with and without P.E., but the flat region is wider with P.E. than without P.E. (4) From the viewpoint of charge control, with P.E. Structure 1 is the best. We conclude that P.E. provides an FET with better performance.

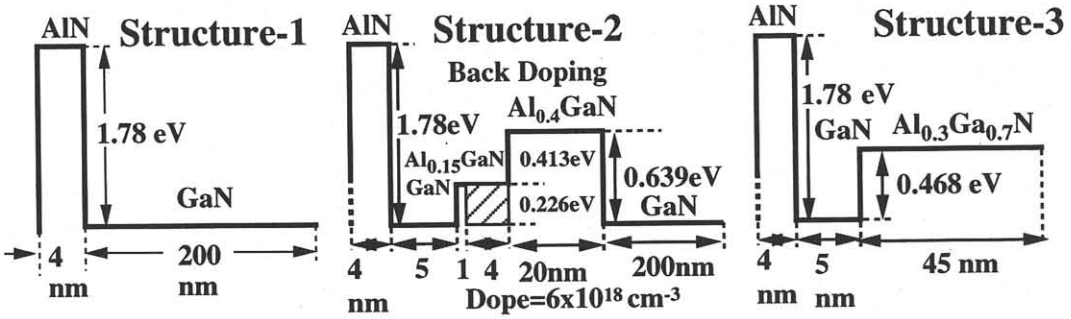

Fig. 1 Three vertical structures used in the simulations.

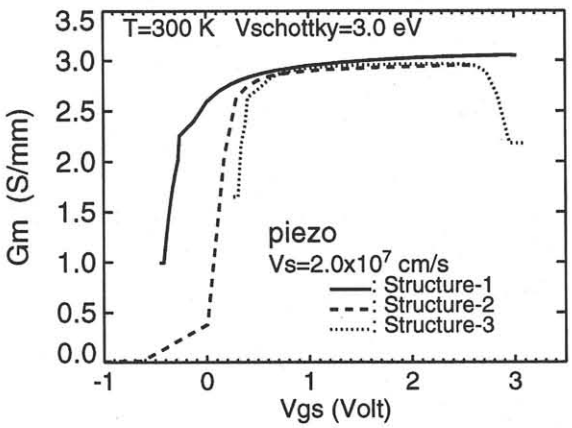

Fig. 2 G_m–V_{gs} characteristics with P.E.

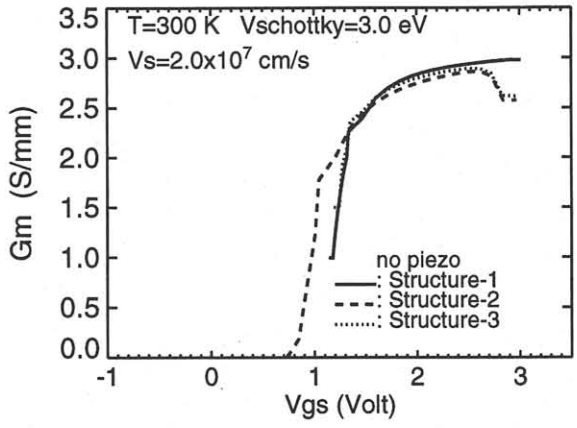

Fig. 3 G_m–V_{gs} characteristics without P.E.

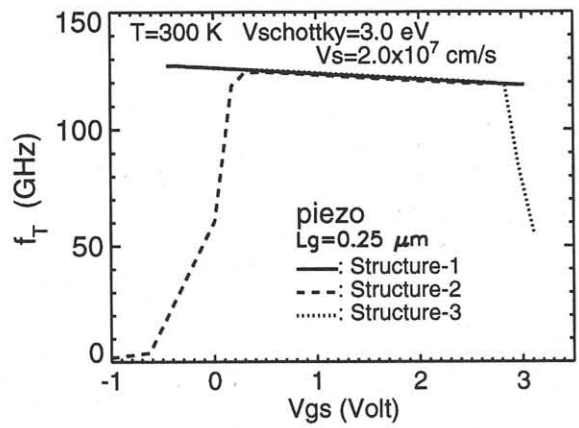

Fig. 4 f_T–V_{gs} characteristics with P.E.

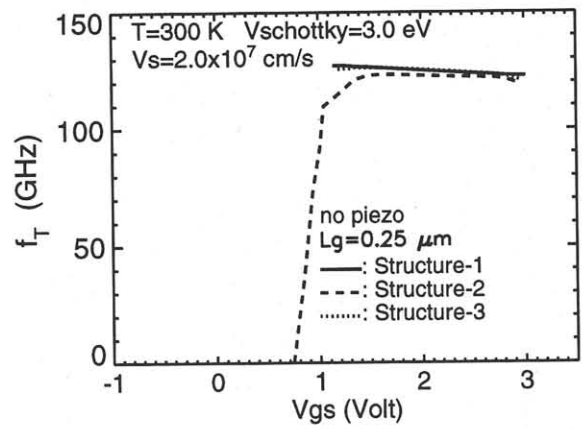

Fig. 5 f_T–V_{gs} characteristics without P.E.

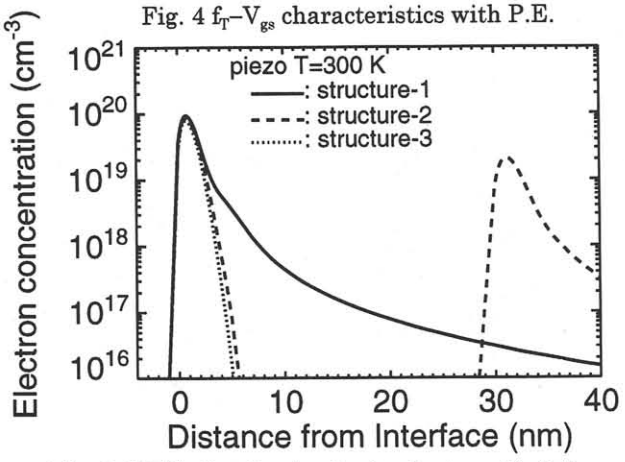

Fig. 6 2DEG distribution in the device with P.E.

References

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