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GaAs MISFET Based Memory with a Nanocomposite Gate

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1. Introduction

Recently, single silicon MOSFET memory structures have been described using threshold voltage changes achieved by charge injection onto a silicon nanocrystal floating gate, buried in the gate oxide between the channel and a continuous control gate [1]. High quality gate dielectrics are required for this technology, as the barriers must be thin enough to allow controlled tunnelling between the nanocrystals and the channel. However, any defect in the dielectric results in an ohmic contact between the gate and the channel and so prevents operation. In contrast, similar defects in the case of GaAs based transistors result only in a Schottky barrier and so operation is maintained.

2. Device Structure

In this paper, a depletion mode δ-doped GaAs MISFET based approach to nanocrystal memories is described. The gate dielectric is formed using oxidised aluminium layers and the nanocrystals are formed using ionised beam deposition of AuPd, which forms 2nm sized islands with high density. Similar islands have previously demonstrated Coulomb blockade in a lateral transistor structure at 77K [2].

The layer structure is shown in schematic cross-section in Fig. 1. The dielectric layers are about 5nm in thickness, formed by room temperature oxidation of 5nm thick layers of deposited aluminium. The control gate metalisation is aluminium.

3. Results and Discussion

Oxidised aluminium is effective as a dielectric in realising δ-doped GaAs based MISFET devices. MISFET transistor characteristics, for a device without nanodots, are shown in Fig. 2. The pinch-off characteristics for the MISFETs are modified from those for conventional Schottky gates by a shift in threshold voltage to more negative gate voltages.

The presence of the metal islands in the gate dielectric strongly modifies the room temperature C-V characteristics of the structure for voltages close to the pinch-off of the channel, see Fig. 3. An excess capacitance can be seen for the structure with nanodots compared to a similar structure without nanodots. The excess capacitance appears at gate voltages between pinch-off and about 2V of further reverse bias, as indicated by the drain current. The excess capacitance is consistent with each nanodot contributing a capacitance of about 0.1aF.

Memory operation, using the threshold shift of a wide channel width transistor, is achieved at 77K, see Fig. 4. A threshold shift of about 1.4V was achieved by sweeping the gate voltage between -3V and 1V for a drain voltage of 0.25V. Tunnelling takes place between the nanodots and the channel, despite similar dielectric thicknesses being formed between the nanodots and the channel or the nanodots and the gate metal. Operation at room temperature in our device is prevented at present because of increased leakage through the aluminium oxide thicknesses used in this experiment.

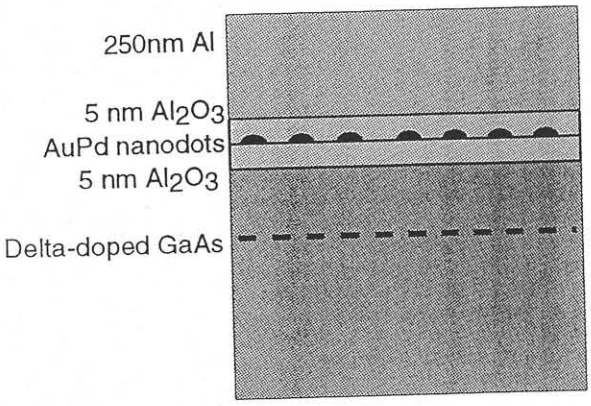

Fig. 1. Schematic cross-sectional diagram of the nanocomposite gate δ-doped GaAs MISFET structure.

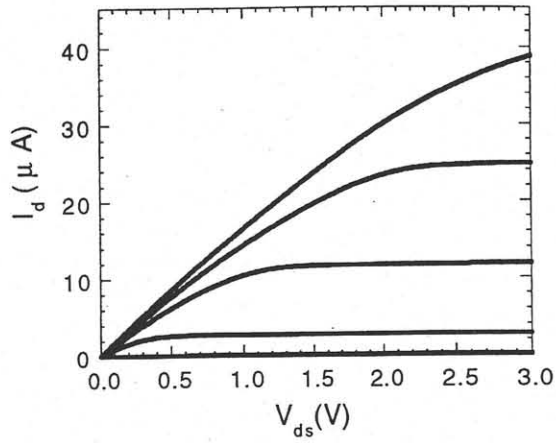

Fig. 2. MISFET transistor characteristics for a large area device without nanodots at room temperature.

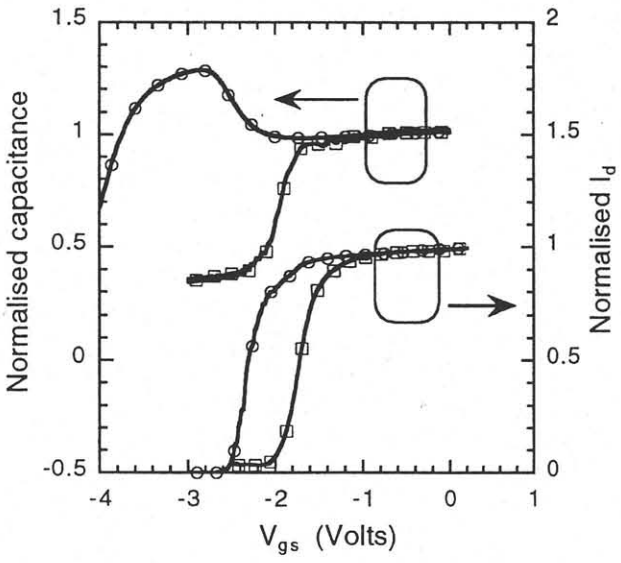

Fig. 3. Normalised capacitance and drain current characteristics for large area devices with (circles) and without (squares) nanodots.

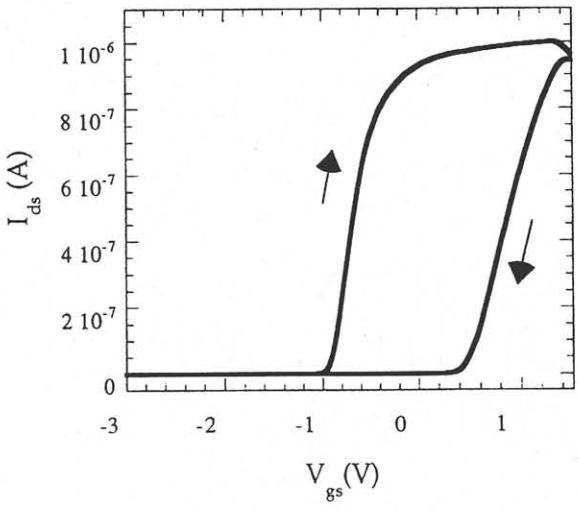

Fig. 4. Drain current hysteresis for a wide channel device measured at 77K. The gate voltage is swept between -3V and 1V in the directions indicated by the arrows.

References

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2. W. Chen and H. Ahmed, J. Vac. Sci. Technol. **B15**, 1402 (1997).

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