Buried Insulator Engineering for sub-0.05μm Fully-Depleted SOI-MOSFET to Reduce the Drain Induced Barrier Lowering

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Abstract The influence of the buried insulator structure on DIBL is analyzed for sub-0.05μm FD-SOI-MOSFET. It is found that a low-ε_r buried layer is effective to reduce DIBL.

1.Introduction

SOI-MOSFET has greast advantages for low power and high speed application, a small parasitic capacitance and a small body bias effect. To miniaturize a fully depleted SOI-MOSFET, SOI thickness should be reduced for decreasing the horizontal drain field which degrades the device characteristics. As the SOI thickness decreases, the influence of the electric field through the SOI layer (fig.1a"A") decreases. However, this leads to an increase in the contribution of the electric field in the buried insulator (fig.1a"B"). Therefore, the influences of the buried insulator structure on the device characteristics are analyzed in this paper, by using two dimensional device simulator. The thickness T_{BOX} and the dielectric constant ε_r of the buried insulator are varied systematically, with including ε_r =1.0 which assume a buried air gap structure as shown in fig.2.

2.Horizontal electric field reduction

Figure 3 shows the calculated threshold voltage variation for the change of V_D from 0.1V to 1.0V (ΔV_{th}) for L=0.04μm. ΔV_{th}decreases with ε_r decreasing. ΔV_{th} strongly depends on T_{BOX} for large ε_r, and weakly for small ε_r. For ε_r=3.9 (SiO_2), ΔV_{th} decreases drastically in T_{BOX} < 100nm. This ε_r requires T_{BOX} < 100nm to cut the field pass "B" sufficiently, since the field pass is mainly distributed at the vicinity of SOI back interface in the buried insulator. On the other hand, a small ΔV_{th} is achieved for low ε_r even when T_{BOX} is large. A low-ε_r structure sufficiently reduces the influence of the field "B" located just beneath the SOI layer, even for large T_{BOX}. This indicates that a device having low ε_r does not require small T_{BOX}. The rate of ΔV_{th} reduction by low ε_r is large for thin SOI device (T_{SOI}=5nm), since the contribution of field "B" is relatively large. When T_{BOX} is very small (e.g. T_{BOX} =20nm), ΔVth weakly depends on ε_r. However, low-ε structure even have an advantage that the parasitic capacitance is small.

Figure 4 shows that ΔV_{th} can be separated into two components, a contribution of field "B" which depends on the buried layer structure, and that of field "A" which is independent of the buried layer structure. Figure 5 shows the electrostatic coupling between the drain and the channel C_{cd}[1], which is the sum of C_1 and C_2 in fig.1b. For ε_r=3.9 (buried oxide), C_{cd} drastically decreases as T_{BOX} decreases, and for ε_r=1.0, C_{cd} is almost independent of T_{BOX}. The results of figs. 4 and 5 agree well with the above discussion on fig.3. They indicate that the ΔV_{th} reduction by low-ε structure can be attributed to the reduction of horizontal electrostatic coupling in the buried layer (C_2 in fig.1b), which is achieved by reducing the dielectric constant in the pass of field "B".

3.Device characteristics

The above results show that the ε reduction is efficient for reducing the drain induced barrier lowering (DIBL) without using very thin buried oxide, which increases parasitic capacitance. The device characteristics for buried air gap device are simulated for an example.

Figure 6 shows the V_{th} dependence on L, and fig.7 the S dependence on L. the solid lines show the results for buried air gap of 400nm thick, and the broken lines the buried oxide of 400nm. The acceptor concentration for T_{SOI}=5nm is $5\times10^{18}cm^{-3}$ and that for T_{SOI}=10nm is 2.5×10^{18} cm^{-3}. For the low power and high speed operation, S factor improvement (steep transition from OFF to ON) and DIBL reduction (small V_{th} change for V_D variation) is very important to achieve high ON/OFF rate. The L limits where ΔV_{th} /ΔV_D becomes 0.1 are shown in fig.8. The improvement made by buried low-ε layer, especially by the buried air gap structure, is remarkable. Figure 9 shows the I_D for the devices where V_{th} are set to achieve I_{off}=10nA/μm @V_D=0.5V for L=0.05μm. The small DIBL and steep subthreshold achieved by the buried air gap structure result in an improvement of ON current.

4.Conclusion

The influence of the buried insulator structure is simulated. It is found that the low-ε buried insulator devices achieve excellent characteristics in the sub-0.05micron region, without using thin buried oxide which increases the parasitic capacitance.

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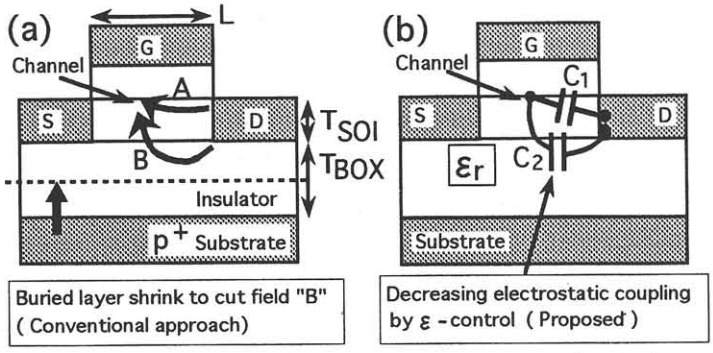

Fig.1 Buried layer Engineering. Arrow "A" represents the drain field through the SOI layer, and "B" through the buried layer. Capacitance C_1 and C_2 the electrostatic coupling corresponding to "A" and "B", respectively.

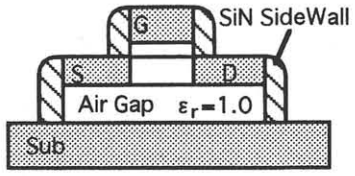

Fig.2 A possible buried low ε layer structure. The buried oxide of conventional SOI wafer is removed by wet etching after forming S/D. A porous SiO_2 buried layer in the bonded wafer is also considered to be possible.

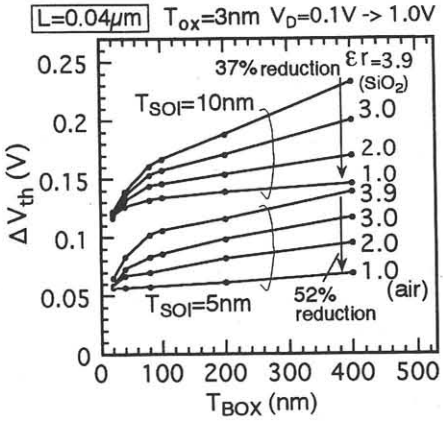

fig.3 Δ V_{th} dependence on T_{BOX}.

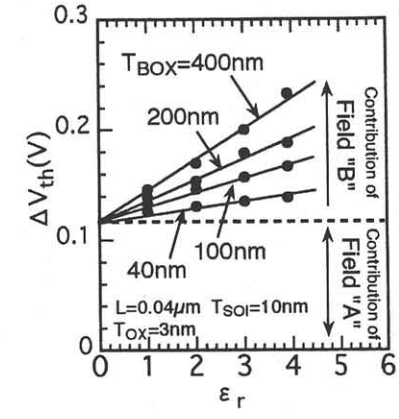

Fig.4 Δ V_{th} dependence on ε .

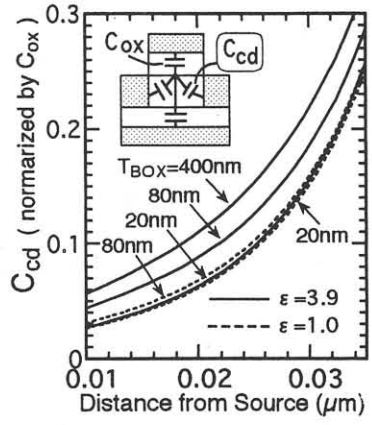

Fig.5 The Capacitance between the drain and the channel.

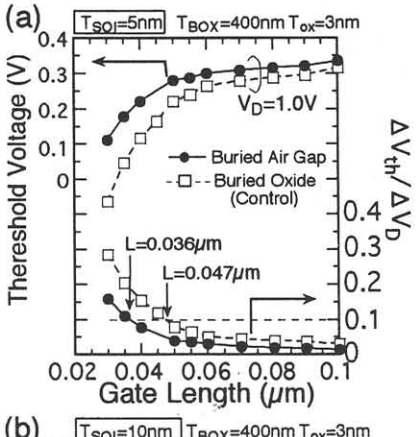

Fig.6 V_{th} dependence on L

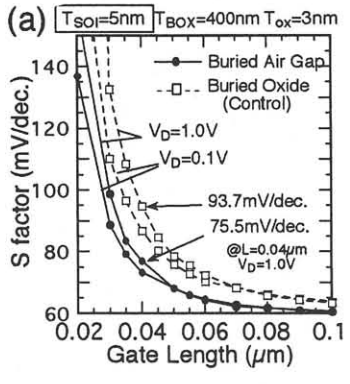

Fig.7 S dependence on L

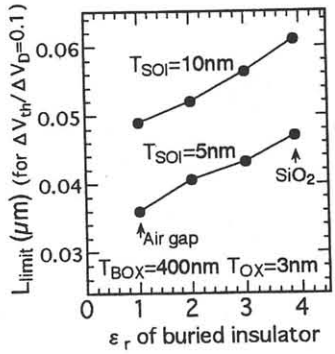

Fig.8 DIBL limit dependence on the buried layer structure.

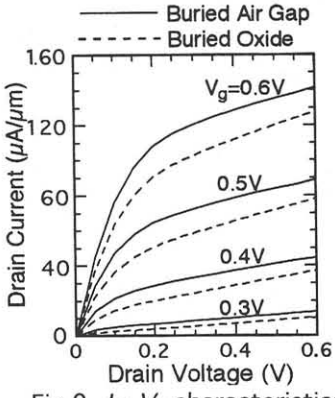

Fig.9 I_D- V_D characteristics.