# A Novel Shallow Trench Isolation with Mini-Spacer Technology

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In this work, we propose a new shallow trench isolation process with a mini-spacer formation before shallow trench etch. With this mini-spacer, thicker corner liner oxide and T-shaped trench can be formed simultaneously. The STI corner oxide-recess was reduced and larger process window for subthreshold kink free device obtained. The isolation capability and junction integrity were both improved as compared with those of the conventional STI process. The gate oxide integrity was also enhanced. This technology was employed for 0.13 um CMOS device fabrication.

## 1. Introduction

Shallow trench isolation (STI) technology has been widely used for sub-0.25 um CMOS devices to achieve higher isolation performance than that of the conventional LOCOS structure. Many papers have described that the corner rounding is the key issue of STI subthreshold kink effect [1]. However, STI corner rounding with recessed refill-oxide still results in parasitic device and broad Vt distribution [2]. If the corner oxide thinning exists, subthreshold kink still occurs even on the rounded corner STI structure. In fact, although a parasitic device exists on the recess-corner of STI, the subthreshold kink effect will not happen on the thicker corner oxide parasitic device which has a higher threshold voltage. On the other hand, a self-aligned T-shaped STI process with a taper trench wall [3] and STI with LOCOS edge [4] were introduced to suppress STI corner oxide recess. In this work, we propose a new shallow trench isolation technology with a mini-spacer formation before shallow trench etching process. With this mini-spacer, thicker corner liner oxide (with a mini-LOCOS bird's beak) and T-shaped trench can be achieved simultaneously providing a larger process window for subthreshold kink free characteristics.

## 2. Experiment

Figure 1 illustrates the process sequence of this proposed shallow trench isolation technology. After pad oxide/SiN deposition and definition, a mini-oxide spacer was formed. High selectivity (oxide/Si) trench etching recipe is adopted. By using a clean step before liner oxidation, this mini-oxide spacer can be removed. After liner oxidation, a thicker corner liner oxide (due to an enlarged corner Si area exposed during liner oxidation) and T-shaped trench (STI width reduced by mini-spacer) was obtained. Finally, oxide refill was employed followed by oxide CMP. After remaining SiN layer removal, this new STI structure is fabricated.

#### 3. Results and Discussion

Figure 2 shows the TEM cross-section of trench profile after oxide refill and subthreshold swing of PMOSFET. Under slightly extended HF deglaze, the conventional STI process has serious subthreshold kink effect; however, this new process shows kink free characteristics even under 3V reverse substrate bias. In contrast to the conventional STI process, this new process enlarges the thickness of liner oxide at the corner to 500A (250A for conventional STI structure) and with 500A bird's beak length. In addition, 150A lateral overcapped-oxide on active region for T-shaped refilled-oxide can be obtained. With these two advantages, the STI corner oxide recess was reduced and larger subthreshold kink free process window can be obtained. Fig. 3 shows the TEM of this new STI corner final profile, with the mini-spacer either removed or not. There is no apparent difference on the STI corner structure (electrical characteristics being the same for both processes). At the same time, other STI isolation

related characteristics were improved with this new STI process. In comparison with conventional STI process (without spacer), the reverse narrow width effect (RNWE) was improved with this new STI process, as shown in Fig. 4. Fig. 5 shows the cumulative plot of inter-well n+ to n-well and p+ to p-well isolation punch-through voltage. With this mini-spacer STI structure, n+ to p+ spacing close to 0.4 um is achieved, which is better than that with conventional process (close to 0.6 um). It is presumably due to a smoother sloped trench profile obtained with this mini-spacer process. Fig. 6 compares the cumulative distribution of junction leakage for STI edge n+/p-well and p+/n-well diodes. With this mini-spacer, junction degradation during Ti-salicidation was suppressed; thus, lower junction leakage was obtained. In addition, the gate oxide integrity (tox = 50 A) of devices with this STI process ( $Q_{BD} = 5.28$  and 5.17 coul/cm<sup>2</sup> for n/p-well, respectively) was improved as compared to conventional STI process. Compared to conventional STI process, the drive current vs. off state leakage characteristics for CMOS with this new STI process have not been degraded, as shown in Fig. 7 (Tox = 50 A, Vd = Vg = 2.5 V, with gate length ranging from 0.18 to 2 um, and W = 10 um). This technology was also employed on 0.13 um CMOS device (with 28A nitrogen-implanted oxide and SiN spacer), as shown in Fig. 8. Well behaved I<sub>D</sub>-V<sub>D</sub> characteristics (Fig. 9) and good subthreshold characteristics (Fig. 10) of 0.13 um MOSFETs were obtained. Excellent current drive, I<sub>D.SAT</sub> of 700 uA/um and 261 uA/um for NMOS and PMOS are achieved with  $I_{OFF} = 6$  and 0.5 nA/um at  $V_{DD} = 1.8 V.$ 

#### 4. Conclusion

A new shallow trench isolation process with a mini-spacer formation was proposed. With this mini-spacer, thicker corner liner oxide and T-shaped trench can be achieved simultaneously providing a larger process window for subthreshold kink free devices.

### References

1) C. P. Chang et al., IEDM Tech. Digest, (1997) p. 661. 2) D. P. Shum et al., IEDM Tech. Digest, (1997) p. 665.

3) P. Fazan et al., IEDM Tech. Digest, (1993) p. 57.

4) T. Park et al., IEDM Tech. Digest, (1994) p. 675.



Fig. 1. Process sequence of new STI process.



a) Poly Si b) Poly Si

Fig. 2. Cross-section TEM of (a) conventional STI and (b) new STI with mini-spacer after oxide refill and Id-Vg characteristics of PMOS, Vd = -0.1V, Vsub = 0~3 V, W = L = 10 um.



Fig. 4. Vt vs. transistor width for STI with mini-spacer and conventional STI.



Fig. 3. Cross-section TEM of STI corner final profile with (a) spacer removed, and (b) spacer not removed before liner oxidation.



Fig. 5. Cumulative distribution of n+ to n-well and p+ to p-well inter-well isolation for new STI with mini-spacer and conventional STI without spacer.







Fig. 8 SEM cross-section of the 0.13  $\mu$ m gate structure (tox = 28A, SiN spacer).



Fig. 9  $I_D$ - $V_D$  characteristics of nand p-MOSFET's.



Fig. 7. Drive current vs. loff for n/p MOSFET (Tox = 50A, Vcc = 2.5V).



Fig. 10 Subthreshold characteristics of n- and p-MOSFET's.