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Improvement of SiO2/4H-SiC Interface by Using High Temperature Hydrogen Annealing at 1000°C

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1. Introduction

Recently, high temperature, high power, and high frequency electronic devices fabricated from 6H- and 4H-SiC have been investigated intensely because of the excellent physical properties of SiC; i.e. high electric filed breakdown strength, high saturated electron velocity, and high thermal conductivity [1]. Especially, 4H-SiC MOSFET is one of the most influential candidates for these devices. However, the channel mobilites of 4H-SiC MOSFETs reported are lower than those of 6H-SiC MOSFETs although the mobility of 4H-SiC estimated from the Hall measurement is higher than that of 6H-SiC [2],[3]. One of reasons of the low channel mobility of 4H-SiC MOSFETs is thought that the interface state density D_{it} is higher than that of 6H-SiC MOSFET.

We have fabricated 4H-SiC MOS capacitors and succeeded in the large improvement of SiO_2/4H-SiC interface by using high temperature hydrogen annealing at 1000℃.

2. Experimental

8° off-angled n-type 4H-SiC (0001) wafers with a n-type epitaxial layer were obtained from Cree Reserch. After the standard RCA cleaning, a sacrifice oxide film was removed by HF solution. A 50nm thick gate oxide film was thermally grown at 1100℃ in dry O_2. Samples were annealed in H_2 (10 torr) at temperatures between 400℃ and 1000℃ for 30 minutes after the oxidation. Aluminum was evaporated on the top of the oxide film and on the back of the sample to make gate electrodes and ohmic contacts of MOS capacitors.

3. Results and Discussion

Fig. 1 shows H_2 annealing temperature dependence of 4H-SiC MOS C-V curves. The dotted line was calculated using the capacitance at 25V as the oxide capacitance and 1×10^{16} cm^{-3} at 200nm in depth as the value of Nd-Na as shown in Fig. 2, where Nd is the donor density and Na is the acceptor density, respectively. The depth profile of Nd-Na was estimated from the C-V curve of the sample annealed in H_2 at 1000℃. In Fig. 1, the measured capacitances at $Vg < -5V$ are lower than the calculated value due to the deep depletion. The measured C-V curve is very close to the ideal C-V one except for the deep depletion region, the hysteresis in C-V curve disappears, and the slope of C-V curve near the flat band voltage V_{fb} is the steepest after H_2 annealing at 1000 ℃. Fig. 3 shows H_2 annealing temperature dependence of the flat voltage shift ΔV_{fb}. The value of ΔV_{fb} hardly changes till 400℃, decreases drastically above 400℃, and tend to saturate around 1000℃. The value of ΔV_{fb} of the sample with H_2 annealing at 1000℃ is 0.64V. These mean that Dit and the negative charges which exist at the SiO_2/4H-SiC interface or in SiO_2 film decrease with H_2 annealing temperature. Fig. 4 shows C-V curves measured by two methods to investigate the effect of H_2 annealing on the distribution of D_{it} in the energy band-gap. The solid C-V curves were measured at f=100kHz , and the dotted C-V curves were measured quasi-statically at the sweep rate of ramp voltage=0.01V/s. The value of D_{it} is described as

$$D_{it} = \frac{1}{e}\left(\left(\frac{1}{C_q} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_h} - \frac{1}{C_{ox}}\right)^{-1}\right). \quad (1)$$

where e is the electronic charge, C_q is the quasi static capacitance, C_h is the capacitance measured at f=100kHz, and C_{ox} is the oxide capacitance, respectively [4]. The difference of capacitance measured by two methods decreases after H_2 annealing at 1000℃, which means that D_{it} was reduced. The distributions of D_{it} in the energy band-gap estimated from eq. (1) are shown in Fig 5 as a function of energy(Ec-E) from the conduction band edge. The value of Dit is underestimated more than about 0.6 eV because the measurement was conducted at room temperature[5]. However, the value of D_{it} after H_2 annealing at 1000℃ is about one-fifth of that of the sample without H_2 annealing. This distribution of D_{it} nearly equals to that of 6H-SiC MOS capacitor [6].

4. Conclusion

We have succeeded in the formation of excellent SiO_2/4H-SiC interface by using high temperature H_2 annealing at 1000℃. The hysteresis in C-V curve disappears, the value of ΔV_{fb} is 0.64V, and D_{it} is reduced to about one-fifth by H_2 annealing at 1000℃ after the oxidation.

References

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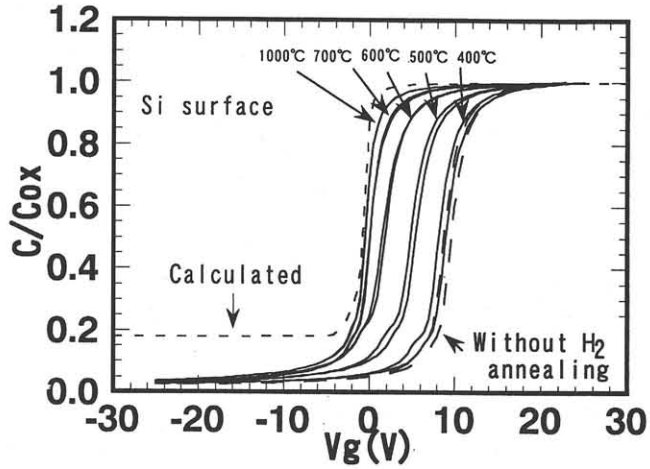

Fig. 1 H_2 annealing temperature dependence of C-V curve of 4H-SiC MOS capacitor. Cox is the oxide capacitance and Vg is the gate voltage.

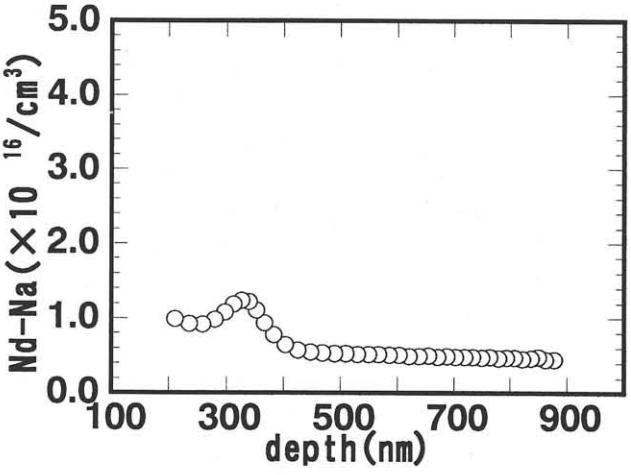

Fig. 2 Depth profile of Nd-Na.

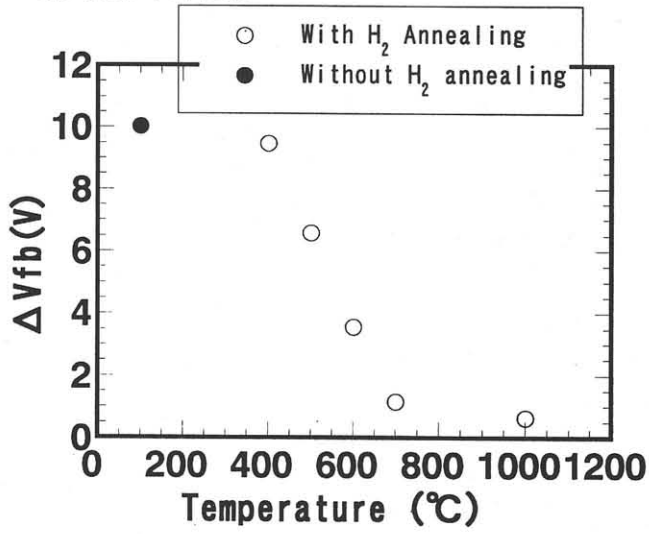

Fig. 3 H_2 annealing temperature dependence of ΔVfb.

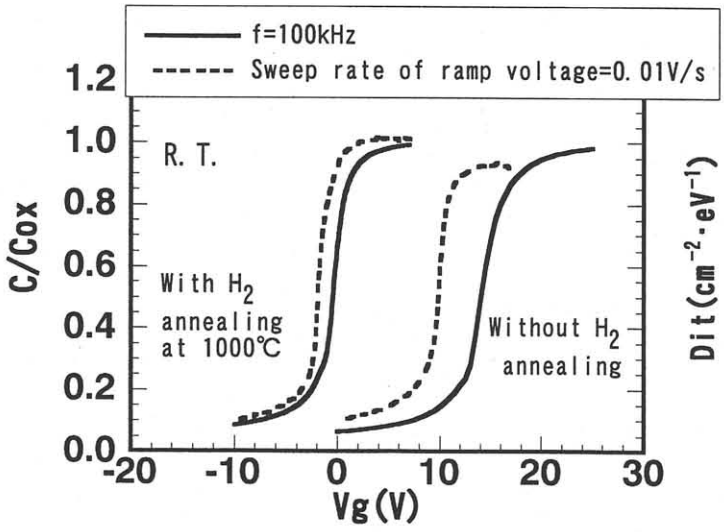

Fig. 4 Effect of H_2 annealing on C-V curves measured at f=100kHz and quasi-statically at sweep rate of ramp voltage of 0.01V/s.

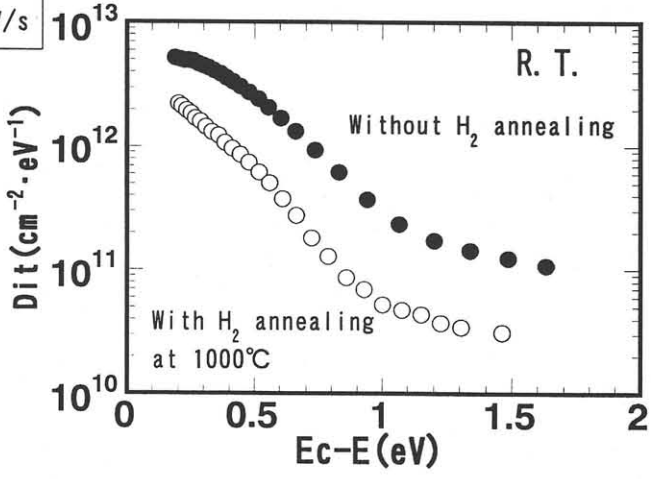

Fig. 5 Distribution of Dit in energy band-gap as a function of energy from the conduction band edge.