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Application of Novel Double-Schottky-Junction AlGaAs/InAs/GaAs Heterostructures for Thermionic-Emitter Hot-Electron Transistors

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1. Introduction

The growth of two-dimensional heterostructures of highly mismatched semiconductor systems by molecular-beam epitaxy (MBE) has long been hindered by the formation of three dimensional islands goverened by the Stranski-Krastanov mechanism. The use of non-(001) surfaces was recently proposed as a novel growth technique for solving this difficulty and in order to achieve a two-dimensional growth for the heteroepitaxial system of InAs/GaAs, which has a lattice mismatch of $\Delta \equiv \delta a_0/a_0$ as large as 7%, (111)A surfaces were used [1]. Despite of the larger lattice mismatch, the interfaces have been confirmed to be atomically flat for both GaAs/InAs and InAs/GaAs, and a network of misfit dislocations is confined at the interfaces [2]. A similar two-dimensional growth was also observed for the more highly mismatched ($\Delta \sim$15%) heteroepitaxy of InSb on GaAs (111)A [3], and this novel growth technique allows the use of much wider combinations of semiconductor materials in the application for heterostructure devices.

Our previous study showed that the Fermi level at both InAs/GaAs and GaAs/InAs interfaces formed on a (111)A substrate is pinned in the conduction band of InAs probably due to the interface states caused by the dislocation network [2]. The InAs/n-GaAs and n-GaAs/InAs heterojunctions are, therefore, expected to show similar vertical transport properties as those of metal-semiconductor junctions. This interface property is important for device applications because both polarities of Schottky junctions (surface-anode type by InAs/n-GaAs and substrate-anode type by n-GaAs/InAs) can only be fabricated by the heteroepitaxy from semiconductor materials.

We propose to apply double-Schottky-junction n-AlGaAs/InAs/n-GaAs heterostructures formed on GaAs (111)A substrates for thermionic-emitter hot-electron transistors, as an example of device applications for this novel MBE growth technique. This kind of hot electron transistor has the advantage of having a low emitter-base resistance compared with the tunneling hot-electron transistor [4-7]. Room temperature operation of this kind of transistor has been confirmed for a number of systems, for example, a metal-base $CoSi_2$/Si [8], an induced-base GaAs/AlGaAs [9], and an AlSbAs/InAs/GaSb system [10].

The AlGaAs/InAs/GaAs system proposed here has the following advantages. First, the high-conduction-band discontinuity of more than 1.0 eV at the emitter-base interface, which is much greater than that of lattice-matched AlAs/GaAs systems, allows stable room-temperature device operation. Second, the metal-deposited InAs surface easily forms good Ohmic contacts because the surface Fermi level is pinned in the conduction band. In addition, this system can be formed on a GaAs substrate, where the majority of optical and electrical devices has been fabricated. Finally, it only needs As as column-V materials to make MBE growth much easier, and does not have the problem of intermixing column-V atoms [11]. We have successfully fabricated novel hot-electron transistors and achieved fairly good room-temperature operations.

2. Results and Discussions

The Schottky-barrier heights at the InAs/n-GaAs and n-GaAs/InAs interfaces formed on GaAs (111)A substrates were measured as 0.62 eV and as 0.54 eV, respectively, from the temperature-dependence of the current-voltage characteristics [12]. This means that the base-collector barrier is slightlly higher than the base-emitter barrier, and that if the transistor was fabricated by n-GaAs/InAs/n-GaAs heterostructures, it would have a poor electron-transfer ratio. In order to improve the transfer ratio, the n-AlGaAs graded layer was used as the emitter leading to the injection of more hot electrons into the collector regions than the n-GaAs/InAs/n-GaAs structures. Figure 1(a) shows the fabricated device structure. The Al composition gradually changed from 0.7 at the interface to 0. The top n-GaAs/AlGaAs layer was selectively etched using an NH_4OH solution and the base ohmic contacts were made by the deposition of TiAu on the InAs-thin films. Using Hall measurements, we found the electron concentration in the n^--GaAs layer which is similarly grown on a semi-insulating GaAs substrate, to be $2\times10^{17}cm^{-3}$. In contrast to the electron concentration, we found the Si concentration to be $4\times10^{17}cm^{-3}$ using SIMS measurements showing a large carrier compensation by the accepter-site Si atoms. The electron concentration in the n^+-GaAs layer was more than $1\times10^{18}cm^{-3}$, which is also highly compensated. For the comparison, the devices with n-GaAs/InAs/n-GaAs structures were also fabricated. The InAs thickness was chosen to be 15 nm and 40 nm. The room-temperature sheet-resistance of the InAs films embed-

ded in the undoped GaAs layers was measured to be 3,000 Ω/sq. (15 nm) and 1,200 Ω/sq. (40 nm).

Figure 1(b) shows the schematic diagram of the conduction band profile of this device. When a negative bias is applied to the emitter relative to the base, the emitter-base Schottky barrier is biased in the forward direction. This injects hot electrons through the base and into the collector. Figure 2 shows the typical common-emitter characteristics obtained at room temperature with a 15 nm-thick InAs film and a graded AlGaAs emitter. The highest common-emitter current gain measured in this device was $\beta \sim 1.1$ at the emitter-collector voltage of 2.5 V. This current gain was reduced for the sample with a thicker InAs film and/or GaAs emitter (Table 1.) because of enhaced electron scattering in the base region and at the base-collector interface. Since the InAs layer becomes highly resistive due to the quantum-size effect when the thinckness is less than 10 nm [2], further improvement in the current gain is difficult to achieve by simply reducing the InAs thickness. It may be possible, however, to use higher emitter-base barriers with the graded emitter with higher AlAs composition and also to optimize the device structures.

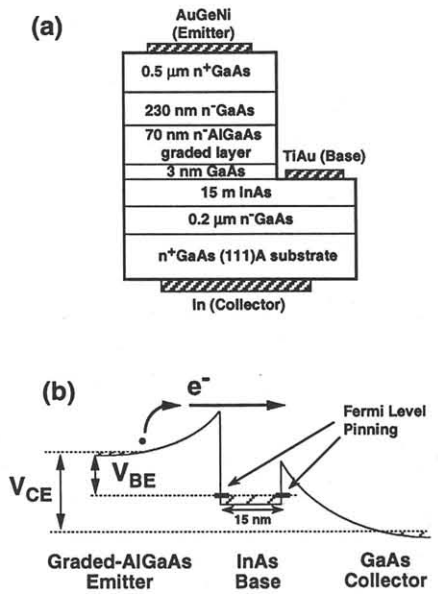

Fig.1 Fabricated structure of AlGaAs/InAs/GaAs hot electron transistors (a) and a schematic diagram of the conduction band profile (b).

3. Conclusion

Double-Shottky-junction AlGaAs/InAs/GaAs heterostructures were applied to fabricate thermionic-emitter hot-electron transistors. The clear room-temperature operation with a common-emitter current gain β of 1.1 was confirmed. This room-temperature operation for thermionic-emitter hot-electron transistors clearly demonstrates the potential device application of the novel growth technique, which drastically improve the film quality in highly mismatched heteroepitaxy.

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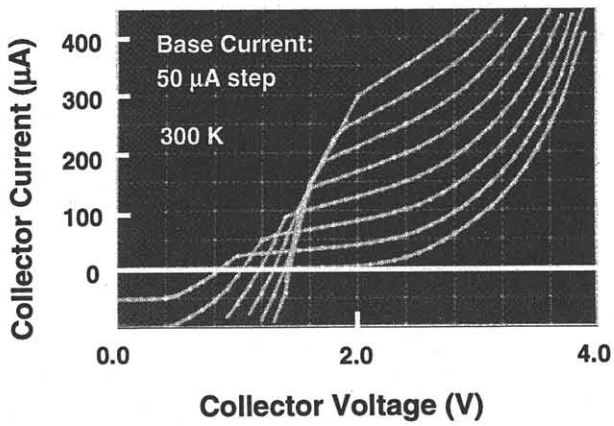

Fig.2: Typical common-emitter characteristics obtained at room temperature. The InAs thickness is 15 nm and the emitter consists of the graded n-AlGaAs.

Emitter Material	*InAs thickness (nm)*	β
graded n-AlGaAs	15	1.1
graded n-AlGaAs	40	0.42
n-GaAs	15	0.18
n-GaAs	40	0.06

Table 1.: Common-emitter current gain β for different InAs thickness and emitter layer composition.