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Doped Channel HFET with Effective Lateral Energy Modulation for High Power Enhancement Operation

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1. Introduction

Doped channel heterostructure FET (DC-HFET) can match many figures of merit of the more established HEMT. Due to the undoped wide band gap barriers [1], DC-HFET can avoid several inherent drawbacks of HEMT. By using the doped channel scheme, instead of the modulation doped one, DC-HFET could attain a better carrier confinement of high carrier density without any real space transfer even under the enhancement mode operation. The DC-HFET reported to date in fact has shown superior characteristics [2] [3] [4]. Nevertheless, an undoped barrier layer commonly buried under the gate electrode inevitably causes large channel series resistance. This series resistance degrades DC characteristics such as transconductance [5], drain conductance and knee voltage, resulting in poor output power characteristics. We have already proposed the laterally modulated energy band structure that can reduce the parasitic resistance. The excellent RF characteristics such as fT of 110GHz and fmax of 200GHz were obtained by our 0.2um gate DC-HFET [6]. The reduction of parasitic resistance can improve the power characteristics as well as the small signal properties. In this paper we demonstrate the effect of our doped channel scheme for power devices. The fabricated devices show excellent RF and DC characteristics superior to that of conventional enhancement HFET.

2. Device structure and Fabrication

In order to reduce the access resistance due to the undoped barrier layer, laterally modulated energy band structure is introduced into the DC-HFET. A schematic cross-section with energy band structures of our DC-HFET is shown in Fig.1. The structure consists of a thick n/n'-GaAs contact layer, an n-AlGaAs intermediate layer, undoped AlGaAs and lightly doped GaAs double barrier layer and a strained n-InGaAs channel grown by Molecular Beam Epitaxy on a S.I. GaAs substrate. The intermediate layer plays a role of achieving both large breakdown voltage and low series resistance. Moreover, it prevents the effect of surface depletion layer between the gate and the source or the drain. Thickness of this layer is optimized to be 10nm doped to $2x10^{18}cm^{-3}$. In the source/drain region, an intermediate layer makes homo junction with the barrier layer. As a result, the conduction band profile connects continuously, with small energy gap between the cap and the barrier layers. On the other hand, the gate is kept isolated because the gate metal is formed on wider bandgap undoped AlGaAs. Therefore, unlike the conventional HFET, low access resistance can be achieved despite the existence of insulator between the contact and channel layers. The thickness of first barrier, i-AlGaAs, is optimized so as to isolate the gate electrode and also to minimize the series resistance simultaneously. The second barrier, lightly doped GaAs, is designed to keep a flat transconductans and to achieve enhancement mode operation. Large gate to channel separation makes the gate capacitance small resulting in good linearity of the device. The devices are fabricated by our standard technology. The 0.6um gate defined by i-line lithography was optimized for high-power use. The surface is passivated with silicon nitride.

3. Results and Discussion

0.6um gate DC-HFET with total barrier thickness of 25nm is designed so as to operate as a full enhancement mode FET for high power use. The InGaAs channel is doped to $1x10^{18}cm^{-3}$. Our structure is effective for enhancement mode FET in which a reduction of channel carrier concentration is required in order to satisfy the enhancement operation. Typical DC characteristics of our enhancement mode DC-HFET are shown in Fig.2 and Fig.3. A large 3-terminal off-state breakdown voltage over 12V (BVgdo=24V), flat transconductance (350mS/mm) and maximum drain current over 300mA/mm (@Vg=1.1V, Ig=100uA/mm) are obtained. The output power characteristics of 9mm-wide DC-HFET were measured using automated tuner system under a drain bias of 3.4V at 1.95GHz. As shown in Fig.4, the device shows the saturation output power of 31dBm with power-added efficiency of 52% and linear gain of 12dB. The device was operated under a near class B operation with bias current of 200mA, corresponding to 10% of Imax. The source impedance was matched so as to extract the maximum power. These excellent characteristics were first demonstrated by our new structure among fully enhancement mode DC-HFETs. These

results suggest that lateral modulation of energy band structure is also effective for the high-power use.

4. Conclusion

We have demonstrated power characteristics of our DC-HFET with effective lateral energy modulation. This structure has an intermediate layer which form homo junction with undoped barrier layer. The fabricated 0.6um gate full enhancement mode DC-HFET shows excellent power performance such as the saturation output power of 31dBm with the power-added efficiency of 52%. These results certify our structure as the effective method to improve the device performance of HFET.

5. References

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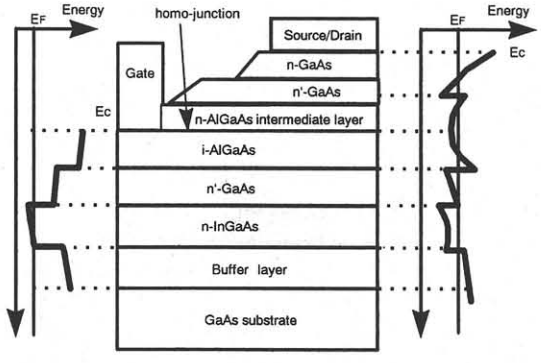

Fig.1 Laterally modulated energy band structure

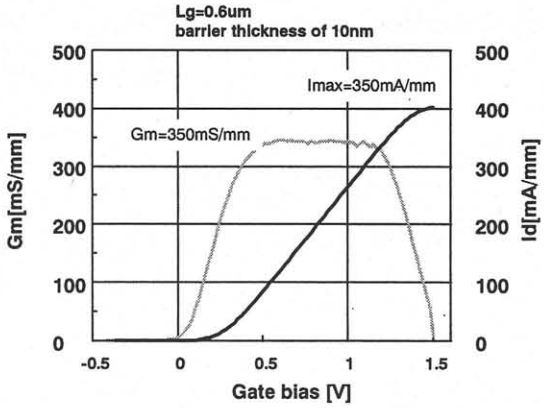

Fig.2 Id,Gm-Vg characteristics

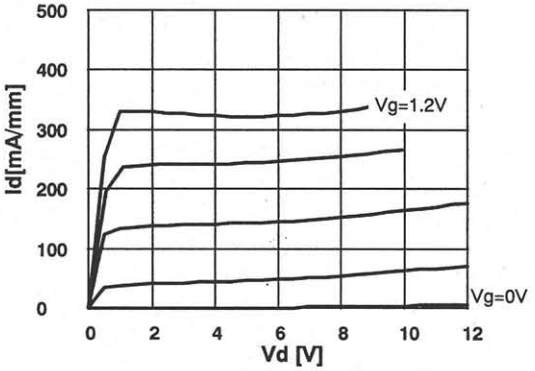

Fig.3 Id-Vd characteristics

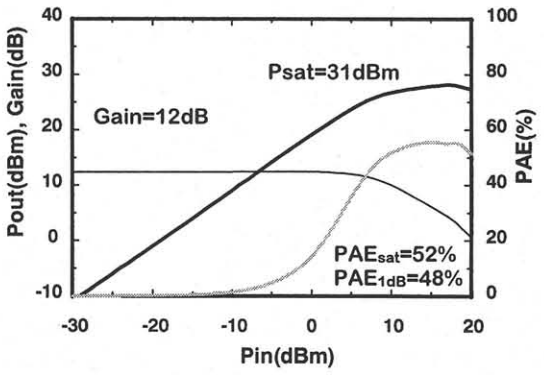

Fig.4 Input-output power characteristics