Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 12-13

Characteristics of Dual Polymetal (W/WNx/Poly-Si) Gate CMOS for 0.1 μm DRAM Technology

Yong-Hae Kim, Sung-Keun Chang, Seon-Soon Kim, Jun-Gi Choi, Sang-Hee Lee
Dae-Hee Hahn, and Hyung-Duck Kim

Semiconductor Advanced Research Division, Hyundai Electronics Industries
San 136-1, Ami-ri, Bubal-eub, Ichon-si, Kyungki-do, 467-701, Korea
Phone: +82-336-630-5146 Fax: +82-336-630-4545 E-mail: yhakim@sr.hei.co.kr

1. Introduction

As the DRAM technology enters into a deep submicron era, the demand for a dual gate is increased to suppress the short channel effect (SCE). It is supposed to be around 0.18 μm periphery CMOS transistor gate length which corresponds to 0.1 μm DRAM technology [1]. As for the chip area reduction a sheet resistance of the gate must be below 5 $\Omega/\square$ [2]. One of the low sheet resistance gate structures, polymetal (W/WNx/Poly-Si) and Ti polycide structure have been reported. But Ti polycide structure shows the linewidth effect which increases the sheet resistance at narrow gate length. Polymetal (W/WNx/Poly-Si) has become a promising gate structure for 0.1 μm DRAM technology.

In this paper, we made the dual polymetal (W/WNx/Poly-Si) gate CMOS down to 0.15 μm gate length.

2. Experimental

The process sequence for dual polymetal (W/WNx/Poly-Si) gate CMOS is as follows: Shallow trench isolation (STI) is followed by shallow well and channel ion implantation. After 45 $\AA$ gate oxidation, 900 $\AA$ amorphous Si is deposited. And boron and phosphorus are implanted for n^+ and p^+ gate respectively. Then 100 $\AA$ WNx and 500 $\AA$ W are deposited by sputtering. The gate capping for self aligned contact (SAC) is made by PECVD SiN. Before the gate patterning we process 600 $^\circ C$ annealing.

The 248 nm KrF lithography is used for the gate patterning with an antireflective layer and the photoresist over-exposure technique. Fig. 1 shows a SEM image of the polymetal (W/WNx/Poly-Si) structure with 0.12 μm gate length. A shallow source and drain extension, 600 $\AA$ sidewall formation are followed by deep source and drain implantation. The rapid thermal annealing (RTA) is used for the source and drain activation.

3. Results and Discussion

Fig. 2 shows the I_D-V_G characteristics of 0.15 μm nMOS and pMOS. The subthreshold characteristics are observed with 86 mV/dec for nMOS and 84 mV/dec for pMOS. Fig. 3 shows the I_D-V_D characteristics. The saturation current of 300 $\mu A/\mu m$ is obtained for nMOS and 110 $\mu A/\mu m$ is observed for pMOS. The C-V curves for the miller capacitor are shown in Fig. 4. The C-V curve of nMOS is well behaved and have C_{INV}/C_{MAX}=95 % which is 5 % improvement comparing to that of n^+ doped poly gate (Fig. 4(b)). However, C_{INV}/C_{MAX} in pMOS is 83 % which means the large gate poly depletion.

Recently B. Yu et al. has derived a relation between the gate poly depletion and the device characteristics [3]. The saturation current (I_{DSAT}) degradation and the effective gate oxide thickness (T_{ox}^{eff}) owing to the gate poly depletion are approximated as follows.

$$\frac{I_{DSAT}}{I_{DSAT}(Ideal)} = 1 - \frac{\Delta V_{gd}}{V_{DD} - V_T}, \frac{T_{ox}^{eff}}{T_{ox}} = 1 + \frac{\epsilon_{ox} X_{gd}}{\epsilon_{si} T_{ox}} \quad (1)$$

Fig. 5 shows the effective gate oxide thickness and the saturation current degradation with the gate poly doping densities. The gate poly doping must be above 5E19/cm^3 to obtain 90 % of the ideal saturation current.

The threshold voltage roll off of nMOS and pMOS is shown in Fig. 6. The short channel effects are effectively suppressed to 0.15 μm gate length and there is no indication of boron penetration.

Fig. 7(a) shows the drain junction leakage current with the post gate oxidation splits. When the post gate oxidation is skipped, the drain junction leakage current is increased by 2 orders at 6V due to the enhanced gate induced drain leakage (GIDL) current. The GIDL current is another issue as well as the gate leakage current [2] when we skip the post gate oxidation. We simulate the GIDL current involving band to band tunneling with MEDICI (Fig, 7(b)). The GIDL current is increased by 1 order in case of skipping the post gate oxidation. Fig. 8 shows the GIDL current with LDD implant energies (a) and doses (b). For the suppression the GIDL current, the LDD implant dose lowering is more effective than the LDD implant energy change. But we need to optimize the LDD implant dose because the saturation current is decreased with the LDD implant dose lowering.

4. Conclusion and Summary

We made the dual polymetal (W/WNx/Poly-Si) gate CMOS down to 0.15 μm gate length. The short channel effects are effectively suppressed and the boron penetration is not observed with pure SiO_2 gate dielectrics. The GIDL current could be drastically suppressed by the LDD dose optimization.

References

[1] K. N. Kim et al., Electron Devices **45**, 598 (1998).
[2] Y. Hiura et al., IEDM, 389 (1998).
[3] B. Yu et al., Electron Devices **45**, 1253 (1998).

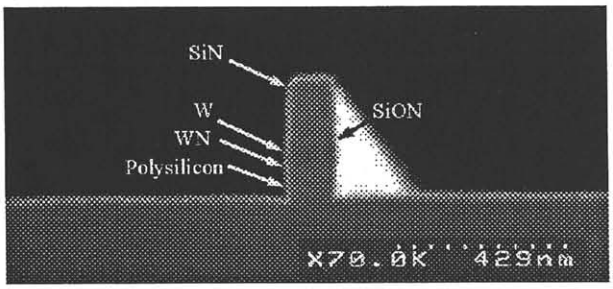

Fig. 1. SEM image of the polymetal (W/WNx/Poly-Si) structure with 0.12㎛ gate length.

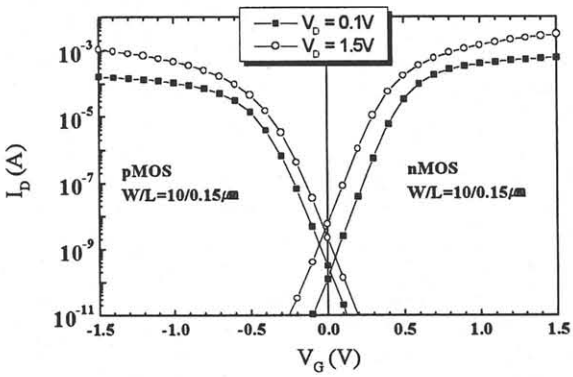

Fig. 2. I_D-V_G characteristics of 0.15㎛ nMOS and pMOS.

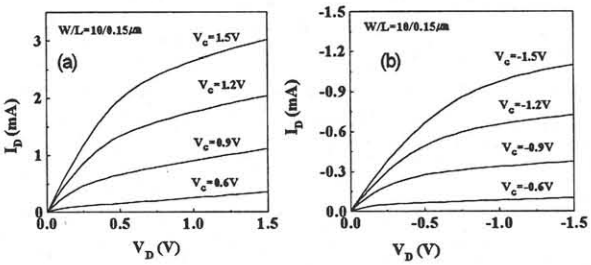

Fig. 3. I_D-V_G characteristics of 0.15㎛ nMOS (a) and pMOS (b).

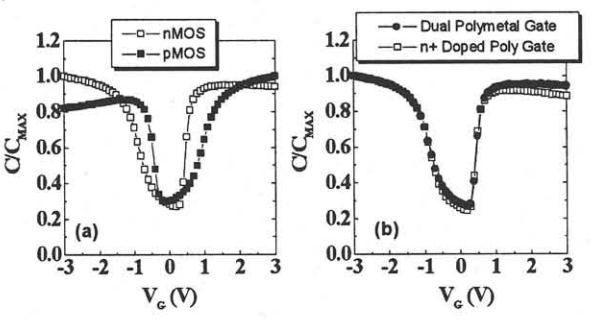

Fig. 4. The C-V curves for the miller capacitor of (a) nMOS and pMOS in dual polymetal gate, (b) nMOS in dual polymetal gate (●) and n+ doped poly gate (□).

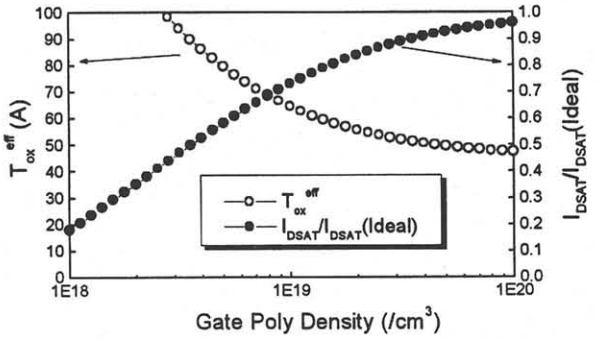

Fig. 5. The effective gate oxide thickness (○) and the saturation current degradation (●) with the gate poly doping densities.

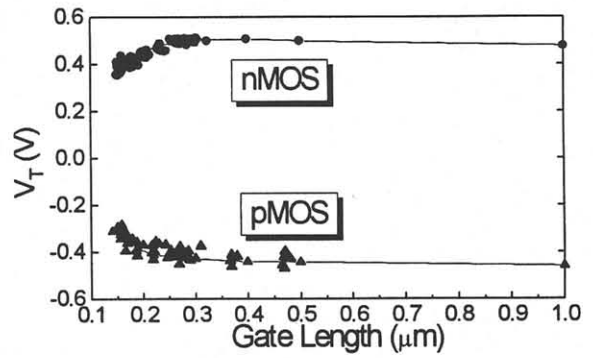

Fig. 6. The threshold voltage roll off of nMOS and pMOS.

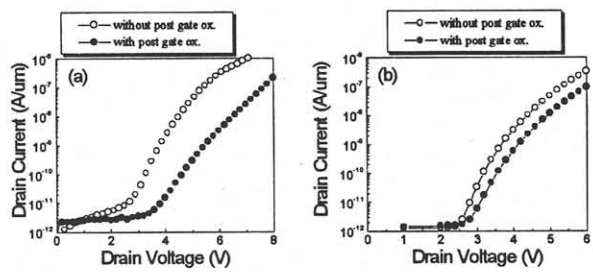

Fig. 7. The drain leakage current with post gate oxidation splits. (a) experimental results, (b) MEDICI simulation.

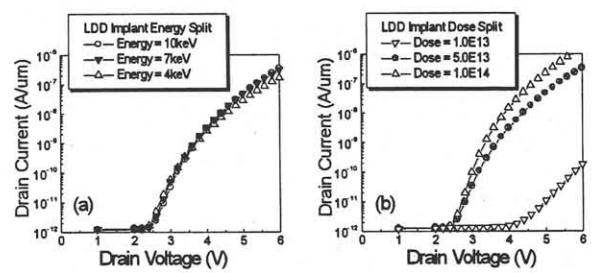

Fig. 8. The drain leakage current simulation with LDD Implant splits. (a) Energy = 4keV, 7keV, 10keV, (b) Dose = 1E13/cm^3, 5E13/cm^3, 1E14/cm^3.