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A New Observation of the Width Dependent Hot Carrier Effect in Shallow-Trench-Isolated P-MOSFET's

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1. Introduction

It was observed that narrow width MOSFET with shallow trench isolation (STI) exhibits severe degradation after hot carrier stress as a result of width reduction. In the case of n-channel MOSFET, it was reported that the hot carrier degradation in narrower device is resulting from extra hot carrier generation and enhanced vertical field at the STI edge [1-2]. However, the mechanism which causes the channel width dependent hot carrier degradation behavior in p-MOSFET is quite different. A study by Chen et al. [3] presented that the enhanced electron trapping efficiency of the gate oxide in the narrow devices is the key factor for inducing enhanced hot carrier degradation in narrow width p-MOSFET's. In this paper, we propose a new while different width dependent channel shortening effect to explain the enhanced hot carrier degradation in p-channel MOSFET.

2. Device Fabrication and Stress Experiments

The devices used in this study were fabricated with 0.25μm CMOS technology and Shallow Trench Isolation (STI). The p-MOSFET's have the same channel length L= 0.25μm while a varying gate widths from 0.25μm to 20μm. The trench is also optimized to suppress the hump in the subthreshold region I-V characteristics. The gate oxide thickness is 6nm and the device has LDD strucure. Various hot carrier stresses were performed. Among these stresses, V_D is fixed at -4.5V and V_G is varied from -0.6V to -4.5V. Saturation drain current (I_{dsat}) is used to monitor the hot carrier degradation and was measured at $V_G = V_D = -2V$.

3. Results and Discussion

It is well known that three different types of damage (interface states, oxide hole trap, and oxide electron trap) are generated during hot-carrier stress in deep-submicron p-MOSFET[4]. To understand how these damage affect the degradation of devices, hot carrier stress were performed at fixed drain bias of -4.5V with various gate bias. The result is shown in Fig. 1, in which degradation is enhanced for a reducing gate width no matter which gate bias were used for the stress. Also, all devices with different width exhibit a largest I_{dsat} degradation after stress at V_G = -0.6V ($I_{G,max}$ stress) where electron trapping accounts for the degradation under this bias condition. Again, Fig. 2 shows the I_D degradation versus stress time for wide and narrow devices under $I_{G,max}$ stress. A narrower width device exhibits larger I_D degradation and a stronger stress time dependent degradation.

In order to explain the observed degradation as above, the substrate current (I_B) and gate current (I_G) are measured for various channel width p-MOSFET's as shown in Fig. 3. Fig. 4 shows the I_B degradation after $I_{G,max}$ stress. From these results, it suggests that the gate injection current and impact ionization rate are always smaller in a narrower device no matter whether it is before or after the stress. So it could not be the reason why narrower device has larger degradation. There must have another mechanism which induces larger I_D degradation in narrower device. Chen et al. [3] observed that the electron trapping efficiency in narrower device is about three times larger than wider ones. So, they concluded that enhanced electron trapping efficiency of the gate oxide of the narrow devices appears to be the cause of width dependent hot carrier degradation. To check the validity of this conjecture, we performed an edge-FN experiment to show that electron trapping efficiency is not the dominant mechanism for narrow width enhanced I_D degradation. Fig. 5 shows the I_G degradation which exhibits weak width dependency. This result shows that our devices have weak width dependent of the electron trapping efficiency during F-N stress. However, the I_D degradation still shows strong width dependent degradation after hot carrier stress. It was concluded that indeed there is another mechanism responsible for the I_D degradation.

As a consequence, extended from the study in [4-5], we propose a new two-dimensional channel shortening concept to explain the observed the enhanced I_D degradation (as observed in Fig. 2). As shown in Fig. 6, we separate the device into two parts, one is the center part and the other one is the edge part. In the center of the channel, the hot carrier damage region (ΔL_c) is the same for devices with different width. But at the edge, due the the encroachment of the STI, enhanced vertical field, the damaged channel is extended from the drain junction toward the center of the channel, this damaged region is represented by ΔL_e. With the reduction of device gate width, as in Fig. 6(b), this damaged region is much more enlarged for narrower gate width device. In other words, both ΔL_e and ΔW increase with reducing gate width. In order to explain this effect quantitatively, we use a measure of the damaged area by ΔL_{eff}, which is the average channel shortening for different gate width(W) devices. Fig. 7 shows the values of ΔL_{eff} as a function of time with varying device gate width. Again, Fig. 8 shows this ΔL_{eff} as a function of device gate width. This ΔL_{eff} value increases with the reduction of gate with which means the existence of a larger channel shortening effect for narrower gate width device. In short, with the reducing device gate with, the channel shortening effect (or the damaged area-the shaded area in Fig. 6) is much more enhanced and hence exhibits a larger hot carrier degradation.

In conclusion, a new two-dimensional width dependent channel shortening concept is proposed to explain the observed width dependent hot carrier degradation in STI p-MOSFET. This channel shortening effect is a measure of the damaged region inside the channel in both channel and width directions. With the reducing gate width, this channel shortening is enhanced such that the hot carrier stress induced damaged region becomes larger. This is the reason why the I_D degradation is enhanced for devices with narrower gate width and with STI structure. This is a very important reliability issue for the present and future deep-submicron CMOS technologies.

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References

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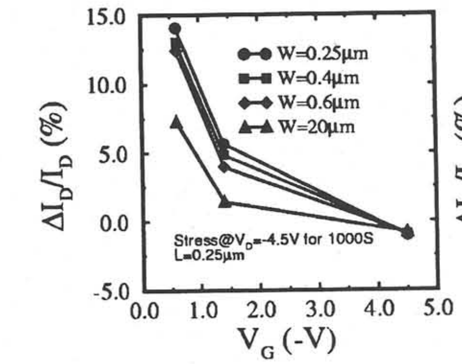


Fig. 1 Drain current degradation after stress at different gate biases. A largest degradation is obsered at $I_{G,max}$.

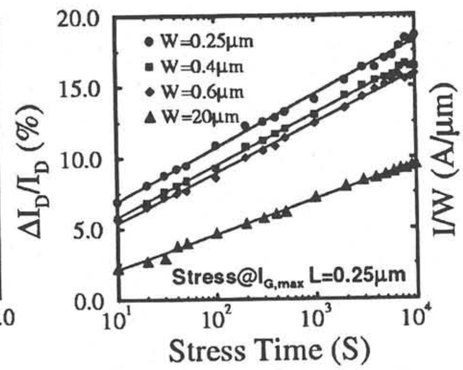


Fig. 2 I_D degradation for different gate width devices after $I_{G,max}$ stress . Narrow width device has larger degradation.

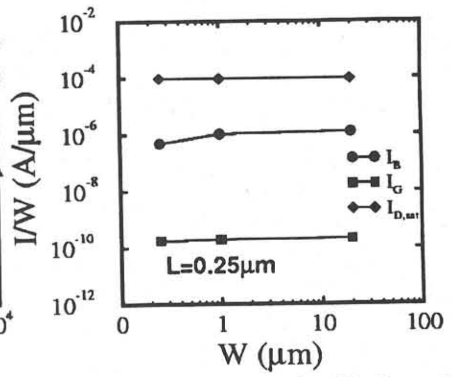


Fig. 3 Comparison of normalized I_B, I_G , and I_D versus width.

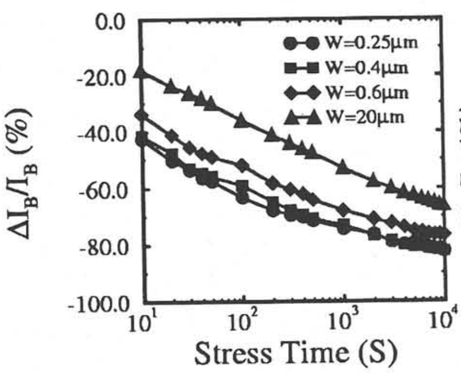


Fig. 4 I_B degradation for various gate width devices after $I_{G,max}$ stress. Narrow width device has larger degradation.

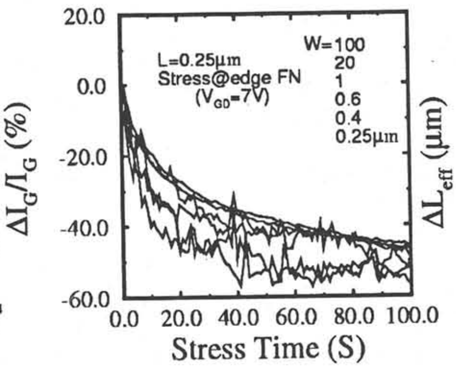


Fig. 5 I_G degradation shows weak width dependence after edge F-N stress.

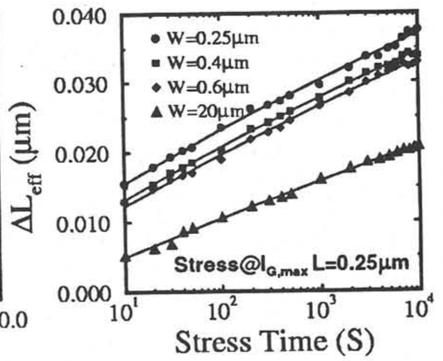
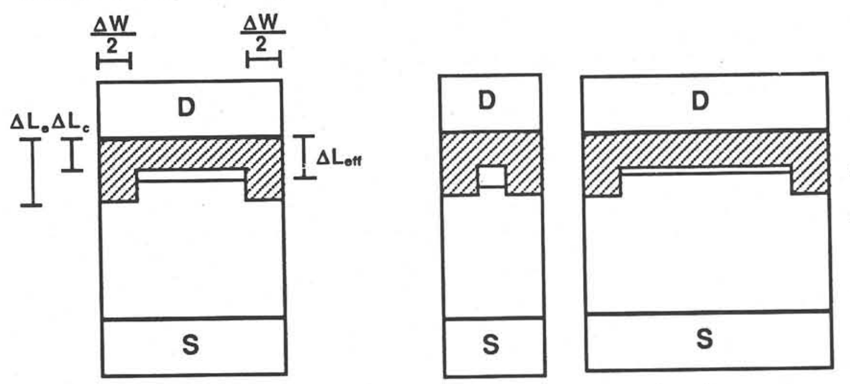


Fig. 7 Time evolution of the calculated effective channel shortening for different gate width devices after $I_{G,max}$ stress.



(a) ΔW, ΔL_c, ΔL_e, and ΔL_{eff} of a device after stress.

(b) Damage area in narrow and wide devices.

Fig. 6 Schematic diagram of the proposed channel shortening effect model. Larger ratio of the damaged region is observed for narrower width device.

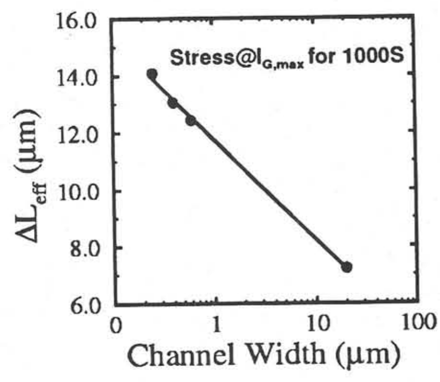


Fig. 8 Calculated effective channel shortening length for devices with different channel width.