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Stress Induced Subthreshold Current Hump in Short Gate-Length pMOSFET's with Shallow Trench Isolation

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1. Introduction

Drain leakage current at zero gate bias has been a major concern in CMOS device scaling. In p-MOSFET's, channel length shortening by negative oxide charge creation during stress can cause an increase of drain leakage current due to enhanced DIBL and punchthrough effects [1-3]. As channel length is further reduced, stress created oxide charge would have a non-localized effect and can result in a significant threshold voltage shift [4].

In quarter-micron CMOS generation and beyond, shallow trench isolation (STI) has been commonly adopted to increase integration density. However, enhanced hot carrier degradation in STI MOSFET's was observed [5,6]. The enhanced degradation is attributed to higher electron trapping efficiency of the gate oxide near the STI edge [5]. In this work, we will report a stress induced subthreshold hump in STI pMOSFET's (Fig. 1). This subthreshold hump may impose a limit on device hot carrier lifetime in short gate-length pMOSFET's with a STI structure

2. Device Characterization

Various gate-length and gate-width pMOSFET's with STI and LOCOS isolation are stressed to investigate the geometrical effect on the subthreshold current degradation. The gate oxide thickness is about 50Å. To enhance the stress effect, an accelerated bi-directional stress (usually occurring in a pass transistor) is used, i.e., a forward mode stress (V_{ds}=-4.3V, V_{gs}=-0.5V) followed by a reverse mode stress (V_{sd}=-4.3V, V_{gd}=-0.5V). In Fig. 2, the pre-stress and post-stress subthreshold characteristics in pMOSFET's with STI and LOCOS structures are shown. The devices have a gate length of 0.25μm and a gate width of 10μm. The measurement drain bias is -0.1V. After bi-directional stress, an obvious subthreshold hump in the STI structure is observed, leading to a large drain leakage current at V_{gs}=0V. In contrast, the hump effect is not shown in the LOCOS isolation device.

3. Gate Width Dependence

The stress induced hump charcateristics in two different gate-width STI pMOSFET's are compared in Fig. 3. The gate widths are 0.3μm and 100μm. The subthreshold humps in the two devices are about the same. In addition, we plot the stress induced drain leakage measured at V_{gs}=0V and V_{ds}=-0.1V versus gate width in Fig. 4. Note that the increased drain leakage current is almost independent of channel width. To explain this result, a schematic representation of a STI p-MOSFET is drawn in Fig. 5. In Fig. 5(a), the hot carrier stressed p-MOSFET can be treated as two transistors in parallel. One is the edge transistor with a gate width $2\Delta W_g$. The other is the center transistor with a gate width $W_g-2\Delta W_g$. After stress, the edge transistor has a larger threshold voltage shift than the center transistor because of the higher electron trapping efficiency at the edge. The total subthreshold current in the stressed pMOSFET is the sum of the currents contributed by each transistor, as shown in Fig. 5(b). Because the edge transistor and the center transistor have different threshold voltage, a current hump in the subthreshold region is obtained. From Fig. 3, it can be deduced that the increased drain leakage current at zero gate bias is predominantly contributed by the edge transistor. As a result, the stress induced drain leakage current is nearly independent of channel width. From Fig. 2(a) and Fig. 3, ΔW_g is estimated to be around 0.1μm.

3. Gate Length Dependence

Fig. 6 shows the gate-length (L_g) dependence of the subthreshold degradation. The stress time is 10^4 seconds. A strong gate-length dependence is observed. The subthreshold hump does not appear in the 0.3μm device. Fig. 7 shows the drain leakage current versus stress time for three different gate lengths. In the L_g=0.22μm device, the drain leakage current increases in the beginning with stress time and then becomes saturated. In the L_g=0.25μm device, the subthreshold leakage remains almost unchanged in the initial period of stress and has a sudden rise around a stress time of 10^3 sec. In the L_g=0.3μm device, we do not observe significant subthreshold leakage degradation in the entire stress period. The above length dependence can be realized as follows. During bi-directional stress, oxide charge grows from both the source and drain junctions towards the channel to a distance L_Q, as illustrated in Fig. 8(a). In relatively long channel devices, ($L_g>2L_Q$), negative oxide charge has only a localized effect and slightly affects subthreshold leakage current by the channel shortening effect. On the other side, if $L_g<2L_Q$ (Fig. 8(b)), negative oxide charge spreads over the entire channel and thus results in a large threshold voltage shift. Therefore, the subthreshold leakage current in short channel devices has a drastical change after stress.

4. Conclusion

The stress induced subthreshold hump in pMPSFET's with STI is investigated. This hump effect appears only when gate length is less than a certain value. Our study shows that the subthreshold hump can increase drain leakage current significantly and imposes a limiting factor in device hot carrier lifetime in short gate-length STI pMOSFET's.

References

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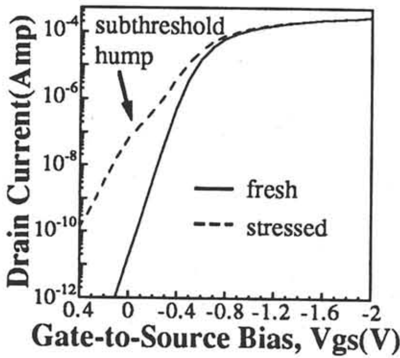
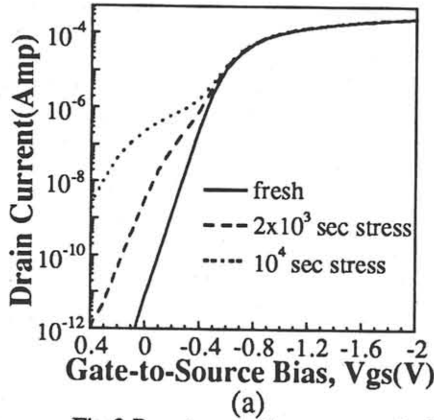


Fig.1 Pre-stress and post-stress I_d-V_{gs} in a STI p-MOSFET. Lg=0.22μm. Stress at V_{gs}=-4.8V, V_{ds}=-0.5V for 3×10^4 sec.



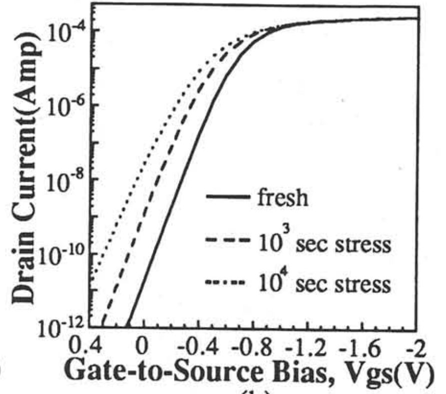


Fig.2 Pre-stress and post-stress I_d-V_{gs} in p-MOSFET's with (a) STI (b)LOCOS isolation. Lg=0.25μm and Wg=10μm. Bi-directional stress is applied.

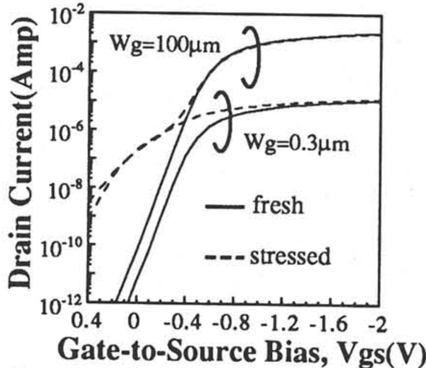


Fig.3 The I_d-V_{gs} characteristics before and after stress in p-MOSFET's with two different gate widths. The gate length is 0.25μm. Stress time is 10^4sec.

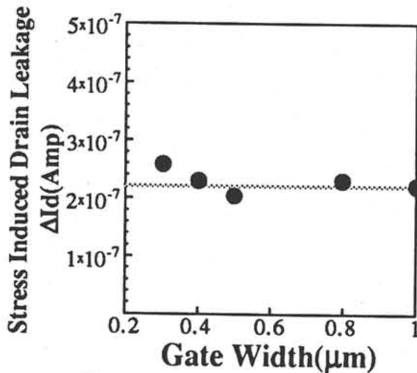
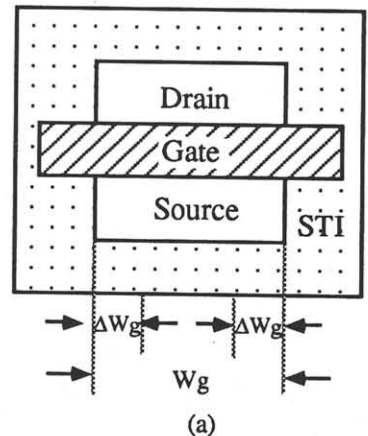


Fig.4 Stress induced drain leakage current at V_{gs}=0V versus gate width. The gate length is 0.25μm.



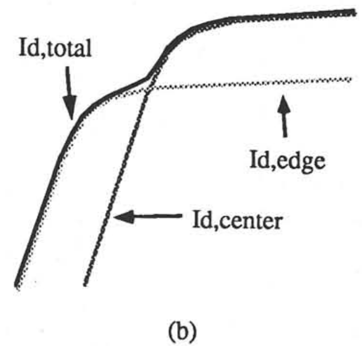


Fig.5(a) The top view of a p-MOSFET with STI. ΔWg represents the width of the edge (b) The total post-stress drain current (Id,total) consists of two components. One is contributed by the edge transistor (Id,edge) and the other is contributed by the center transistor (Id, center).

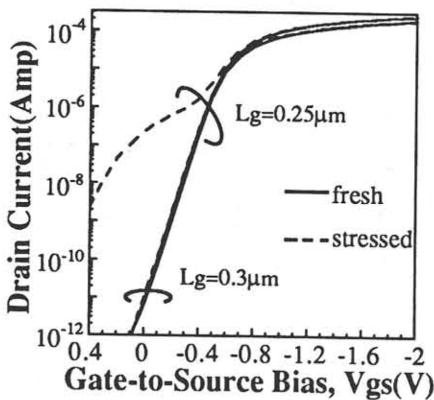


Fig.6 The I_d-V_{gs} characterists before and after stress in STI p-MOSFET's with two different gate lengths. The gate width is 10μm. Stress time is 10^4 sec.

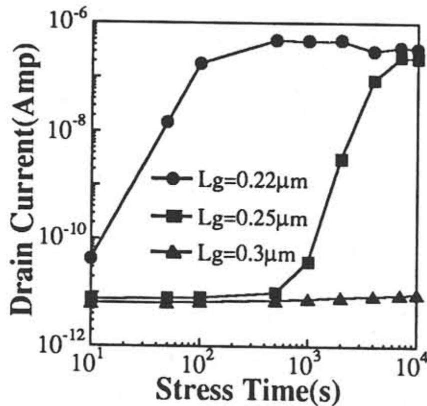


Fig.7 The stress time dependence of drain leakage current measured at V_{gs}=0V and V_{ds}=-0.1V for different gate lengths.

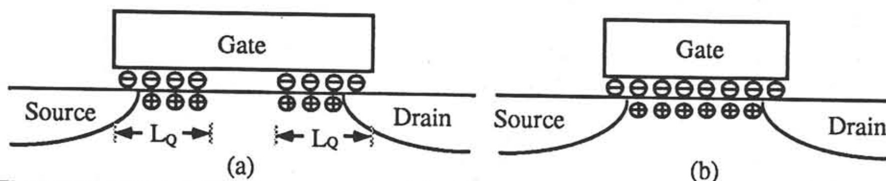


Fig.8 Illustration of the stress created oxide charge distribution in long channel and short channel p-MOSFET's. (a) For $Lg > 2L_Q$, stress created negative oxide charge only has a localized effect. (b) In shorter devices ($Lg < 2L_Q$), negative oxide charge spreads all over the entire channel and lowers the surface barrier height.