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Optimized Shallow Trench Isolation Technology for DRAM Embedded Logic Process

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1. Introduction

Shallow trench isolation (STI) technology has become indispensable for device fabrication according to the quarter-micron device rule to achieve higher scalability and isolation performance. The critical issue in the case of the DRAM embedded logic process is that a higher step height at STI occurs between the DRAM and logic regions because of the difference in the chemical mechanical polishing (CMP) rate between SiO2 and SiN which arises from the difference in the active area density. Moreover, it is necessary to ensure against silicon erosion and polysilicon residue by gate electrode formation. In particular, a dual work function gate is indispensable for high-performance logic, it is difficult to form P+ and N+ gates. Furthermore, it is used to obtain two different gate-oxide thicknesses in the DRAM region and high-performance logic region. To remove the first gate-oxide layer in the logic region, the dip is amplified at the STI top corner by HF solution. The dip leads to the undesirable double hump in the subthreshold IV characteristic and a reverse narrow channel effect (RNCE) [1,2]. To prevent the dip, several approaches of varying complexity have been proposed such as T-shaped STI[3], sidewall protection[4,5] and mini-LOCOS oxidation[6,7].

In this work, we developed an important STI technology which, besides using an optimized active dummy, realized dip-free STI by a SiN recess for the DRAM embedded logic process.

2. STI Process Sequence

Fig.1 shows the proposed STI process for the DRAM embedded logic process. It involves 15nm pad oxidation followed by 200nm thick nitride layer deposition on p-type silicon. The stack was patterned with an active dummy with pattern density nearly equal to that of the DRAM cell, followed by 400nm trench etching and 20nm liner oxidation in 1000 ℃ HCl+O2 ambient after undercutting the pad oxide. Then SiN was recessed by hot phosphoric acid. The recess value was optimized to obtain a flat surface after gate-oxide formation. High density plasma (HDP) CVD oxide was utilized to fill the gap, and densified at 1000℃ for 30min in N2 ambient. Dry-etch-assisted CMP in the wide active pattern was carried out under a condition of high selectivity (SiO2/SiN). After CMP planarization, the SiN film was completely removed. The SEM cross-sectional views of the conventional STI and proposed STI after gate electrode formation are shown in Fig.2(a),(b).

3. Results & Discussion

Fig.3 shows the relationship between the active area ratio and gate poly short yield. The proposed STI has a wide margin for gate electrode formation for a high active area ratio. The Vg-Id characteristics are shown in Fig.4. There is no "double hump" at a reverse substrate bias of 2.0V in both the conventional STI and proposed STI because of the use of the active dummy and the optimized CMP condition. Fig.5 shows the dependence of Vth on channel width for gate lengths of 0.2um and 1.0um. There is no difference in RNCE between 0.2um and 1.0um. The RNCE was significant in the case of conventional STI. The ΔVth (between W=10um and 0.2um) is 77mV for conventional STI. The proposed STI can suppress the RNCE to 56mV, 39mV and 23mV for SiN recess values of 15nm, 46nm and 54nm, respectively. Fig.6 shows the n+/p- junction leakage current in the active area (Ja) and STI peripheral area (Jp). There is no remarkable difference in the junction leakage current between conventional STI and proposed STI. It is shown that in the proposed STI, there is less junction leakage current of the peripheral components than in the conventional STI. This is announced to be because the active area is increased in the conventional STI due to corner recesses. Fig.7 shows the Qbd characteristics for 15nm and 46nm SiN recess conditions. Qbd increases slightly with an increase in the SiN recess value. In the proposed STI, the active edge is covered by liner oxide, but no degradation of the gate oxide is observed. Fig.8 shows the dependence of the threshold voltage on channel width for various active area ratios. It is observed that a higher active area ratio suppresses the RNCE. The active area ratio should be more than 24% for the DRAM embedded logic process.

4. Conclusion

The proposed STI, which is optimized for the DRAM embedded logic process, is presented. A wide process margin of gate electrode formation is obtained and the junction leakage current does not increase. There is no damage to the Si substrate covered with a liner oxide film at the active edge. RNCE is successfully suppressed with increasing SiN recess amount. The proposed STI has good TZDB and Qbd characteristics. Furthermore, the reliability of the gate oxide of the proposed STI is improved over that of the conventional STI structure. This technology should be applied to 0.13um DRAM embedded logic process.

References

[1] Andres Bryant et.al., IEEE Electron Dev.(1993) p. 412.
[2] A.H.Perera et.al., IEDM(1995) p. 679.
[3] T.Ishijima et al., IEDM(1990) p. 257.
[4] Pierre C. Fazan et.al., IEDM(1993) p. 57.
[5] W.K.Yeh et.al., SSDM (1998) p. 98.
[6] A.Chatterjee et al., IEDM(1996) p. 826.
[7] T. Park et al., IEDM(1994) p. 67

- O Pad oxidation 15nm
- O SiN CVD 200nm
- O Photoresist mask with active dummy
- O SiN dry etching
- O Resist removal
- O Trench etching 400nm
- O Liner oxidation 20nm
- ● SiN recess
- O HDP CVD 600nm
- O Photomask open in wide active area
- O SiO2 etching
- O Resist removal
- O CMP planarization
- O SiN removal
- O Sacrificial oxidation 20nm after HF:15nm
- O Multigate oxidation HF:22nm@DRAM, 28nm@Logic
- O Gate electrode formation

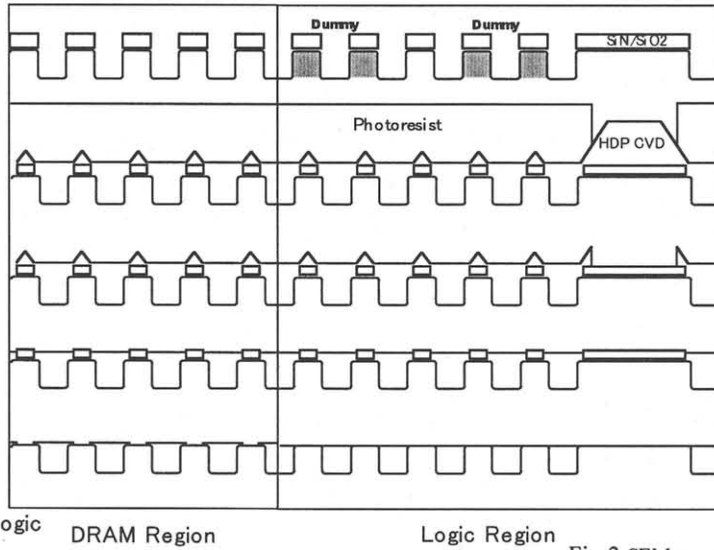
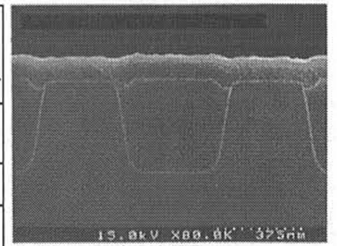
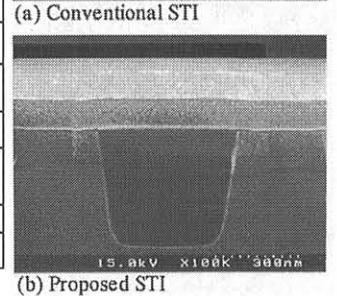


Fig.1 Process sequence of the proposed STI



(a) Conventional STI



(b) Proposed STI

Fig.2 SEM cross-sectional view of conventional STI(a), proposed STI which SiN lateral etch=54nm(b).

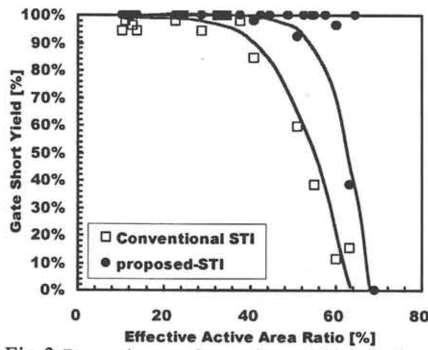


Fig.3 Dependence of gate short yield on active area ratio for conventional STI and proposed STI. Proposed STI has a high yield for a high active area ratio.

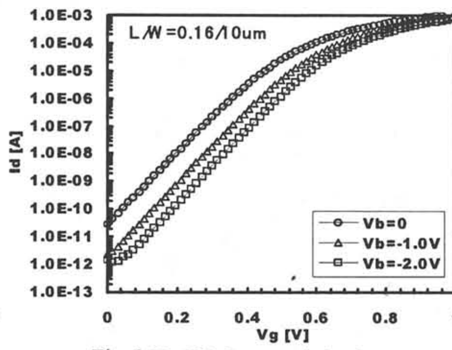


Fig.4 Vg-Vd characteristics for proposed STI. Double hump does not occur. Back Bias=0V,-1.0V and -2.0V.

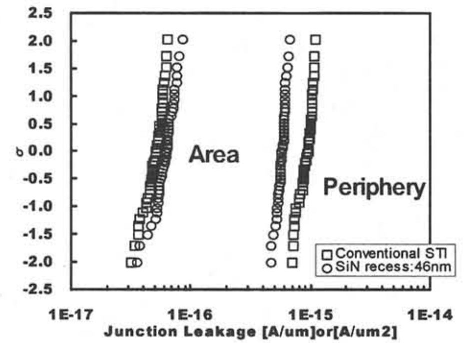
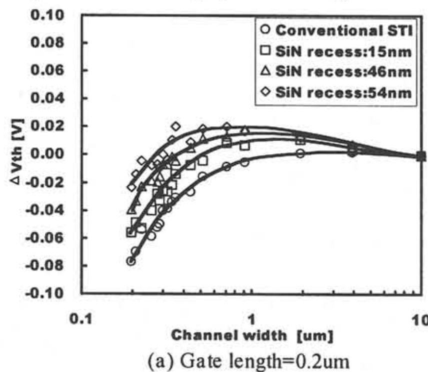
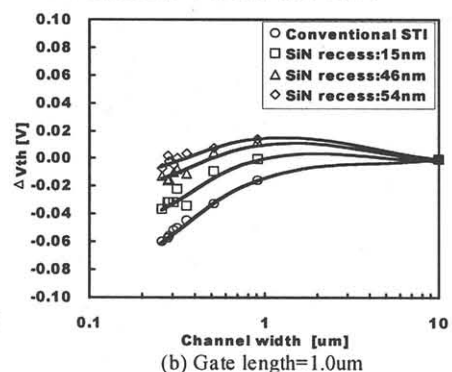


Fig.6 Cumulative distribution of n+/p- area and peripheral diode leakage current at VR=2.5V.



(a) Gate length=0.2um



(b) Gate length=1.0um

Fig.5 Dependence of threshold voltage on channel width. Gate length=(a)0.2um and (b)1.0um for conventional STI and proposed STI, SiN recess value as a parameter.

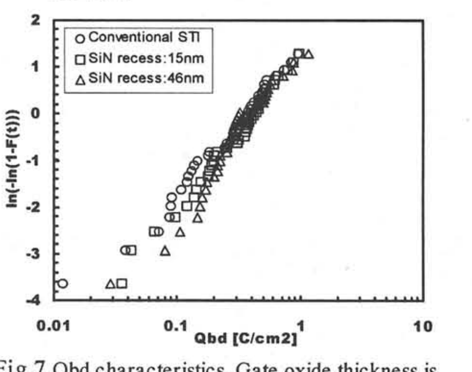
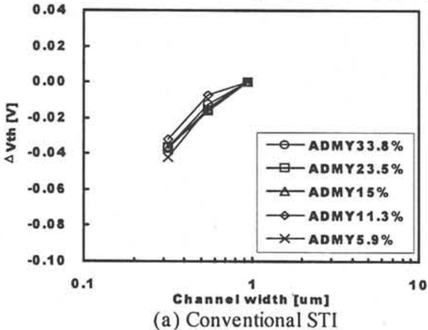
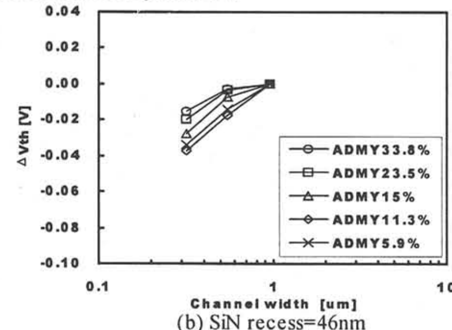


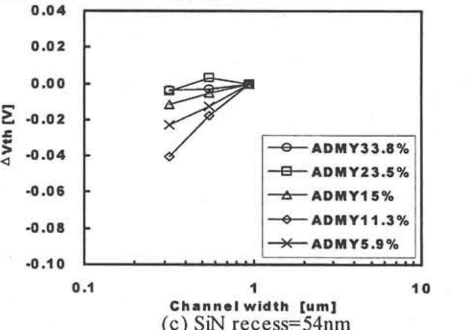
Fig.7 Qbd characteristics. Gate oxide thickness is 3.1nm, as grown. Current density J=-10mA/cm². Gate oxide area is 1.0mm²



(a) Conventional STI



(b) SiN recess=46nm



(c) SiN recess=54nm

Fig.8 Dependence of threshold voltage on channel width for conventional STI(a), SiN recess=46nm(b) and SiN recess=54nm(c), active area ratio as a parameter.