Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 318-319

Modeling of Soft Breakdown in Ultrathin Gate Oxides

Wataru Mizubayashi, Hiroshi Itokawa, Seiichi Miyazaki and Masataka Hirose
Department of Electrical Engineering, Hiroshima University, Kagamiyama 1-4-1, Higashi-Hiroshima 739-8527, Japan
Phone: +81-824-24-7648, Fax: +81-824-22-7038, E-mail: miyazaki@sxsys.hiroshima-u.ac.jp

1. Introduction

The physical modeling of time-dependent dielectric breakdown(TDDB) in ultrathin gate oxides is one of key issues for scaling of MOSFETs. For gate oxides thinner than 5nm, stress-induced leakage current(SILC) appears under constant current or voltage stress. Further stress causes a dramatic jump of the tunnel current, resulting in soft breakdown(SBD)[1-7].

In this paper it is shown that the transition from SILC to SBD occurs when the oxide electric field reaches a critical value independent of oxide thickness. Also, the time to soft breakdown is kept identical regardless oxide thicknesses when the same stress electric field is applied to oxides. An analytic model to explain the observed results is presented.

2. Experimental

MOS capacitors were fabricated on p-Si(100) substrates with LOCOS structures. Si wafers were cleaned by an NH_4OH:H_2O_2:H_2O=0.15:3:7 solution at 80°C for 10 min. Subsequently the surfaces were terminated with hydrogen in a 0.1%HF+1%H_2O_2 solution to minimize the surface microroughness[8]. The gate oxides with thicknesses from 2.5 to 4.9nm were grown at 850°C in dry O_2, and n^+poly-Si gates were formed. Electron injection from the poly-Si gate was employed for constant current or voltage stressing.

3. Results and Discussion

3.1 Time-Zero Dielectric Soft Breakdown

In order to measure a critical oxide electric field at which the tunnel current jumps from SILC to SBD, the gate voltage was ramped up and down at a rate of 40mV/sec to the maximum which was increased by 20mV step for each cycle of voltage scan. The measured current versus oxide voltage curves are shown in Fig. 1, where Voxi indicates the oxide voltage corresponding to the onset of SILC, and Voxc refers to the critical oxide voltage to cause the soft breakdown. As shown in Fig. 2, the soft breakdown field defined by Eoxc=Voxc/Tox, where Tox is the oxide thickness, is in the narrow range 10.7-11.0MV/cm for 3.5-4.9nm oxides. This suggests that there exists a critical oxide field strength at which the soft breakdown is triggered. SILC and SBD have so far been explained by formation of a percolation path via oxide traps generated by voltage or current stress[9-11] or formation of a localized conductive path in SiO_2[2,3]. In Fig. 3 the measured tunnel current after dielectric degradation is compared with the calculated result derived from a proposed model (Fig. 4) which is based on our previous model[3] and modified by percolation path models[9-11]. At the final stage of SILC the conductive region is formed within 1.2nm from the SiO_2/Si interface where strained Si-O-Si bonds due to strong compressive stress could become defect precursors[12,13]. The total area of such conductive region $S_T=\Sigma S_j$ as schematically shown in Fig. 4(a) ranges from ~5% to ~10% of the gate area as shown in Fig. 5(a), indicating that rather homogeneous defect creation occurs during stress. Further increase of oxide field towards Eoxc dramatically enhances the rate of bond breaking[14] and the localized percolation path or conductive path is formed at a particular site as shown in Fig. 4(b), resulting in the current jump to SBD. Two interesting features in SBD are drawn from the result of Fig. 5(b). The areal size of the conductive path S_L is two order of magnitude smaller than S_T and tends to saturate around 80×80nm^2 as Tox decreases to 3.5nm, indicating that SBD is spatially localized breakdown process. The other important is that the remaining oxide thickness tox above the conductive path is kept unchanged at 1.7nm because the SBD current can be sustained by direct tunneling through the 1.7nm thick oxide with an area of S_L without inducing thermal breakdown. Note that in the percolation path model the conduction between two neighbor traps becomes possible when the mutual distance is close to 1nm[9].

3.2 Time-Dependent Dielectric Soft Breakdown

Further insights in the dielectric degradation mechanism can be obtained by time-dependent soft breakdown measurements. McPherson and Mogul[14] have proposed the thermochemical E model to describe TDDB, in which weak bonding states in SiO_2 can be broken by thermal activation process through strong dipolar coupling of intrinsic defects with local electric field. They have shown that the time to failure is determined by the oxide electric field. In order to test this idea, the constant current stress was applied to 2.5-4.9nm oxides by keeping the oxide electric field at 10.5MV/cm which is smaller than the critical oxide field Eoxc or time-zero SBD field as determined in Fig. 2. As shown in Fig.6 the tunnel current under stress or the corresponding gate voltage remains unchanged until SBD occurs. The time to SBD obtained from the Weibull plot, 50%t_{SBD} is shown in Fig. 7 together with the charge to soft breakdown, 50%Q_{SBD} as a function of Tox. It is interesting to note that t_{SBD} is nearly independent of oxide thickness. Namely, under the constant stress current J_{ST} at the identical oxide field strength the soft breakdown of fresh oxides occurs after the identical time t_{SBD} regardless oxide thicknesses. In other words the constant field stress gives the identical time to soft breakdown. On the other hand $Q_{SBD}=J_{ST}\times t_{SBD}$ oscillates when Tox

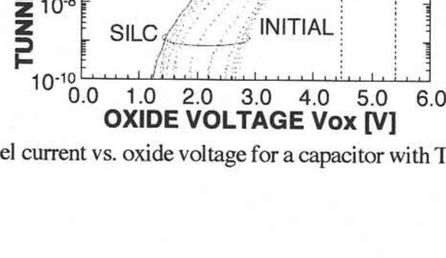

Fig. 1 Tunnel current vs. oxide voltage for a capacitor with Tox=4.9nm.

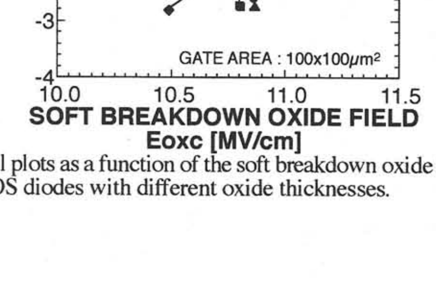

Fig. 2 Weibull plots as a function of the soft breakdown oxide field Eoxc for MOS diodes with different oxide thicknesses.

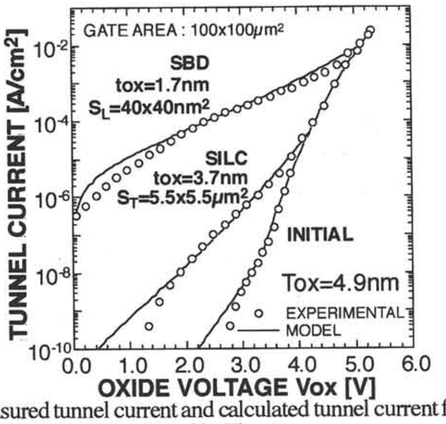

Fig. 3 Measured tunnel current and calculated tunnel current for the MOS capacitor which appeared in Fig. 1.

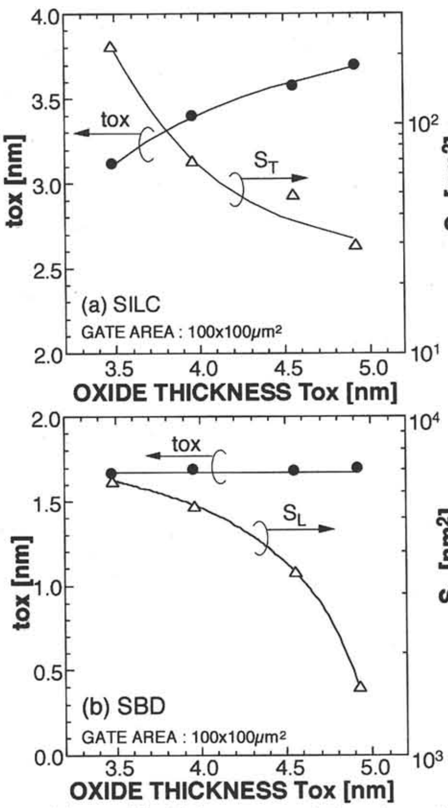

Fig. 5 The remaining oxide thickness tox existing above the localized conducting region obtained from measured I-V curves for SILC (a) and SBD (b) plotted as a function of oxide thickness Tox. S_T and S_L were calculated from the measured SILC and SBD current.

exceeds 3.0nm because the Fowler-Nordheim tunnel current at a given oxide field oscillates with Tox[15]. The result of Fig. 7 implies that the driving force which causes the dielectric soft breakdown is the oxide electric field rather than injected current.

4. Conclusions

It is likely that the dielectric degradation of ultrathin gate oxides occurs through formation of the conductive path or percolation path which might be induced by Si-O-Si bond breaking under oxide electric field. It is also shown that the soft breakdown in ultrathin gate oxides is triggered by the oxide electric field, in consistency with the thermochemical E model[14].

Acknowledgment

Part of this work was supported by the "Research for the Future" Program in the Japan Society for the Promotion of Science (No. RFTF96R13101).

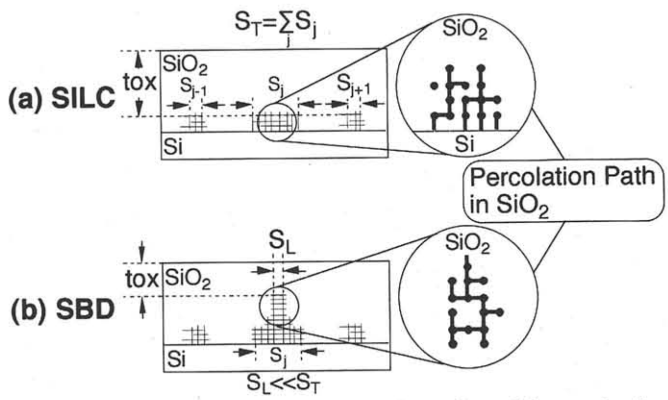

Fig. 4 Schematic illustration to explain formation of the conductive region S_j which induces SILC(a) and formation of the conductive path S_L which leads to soft breakdown(b).

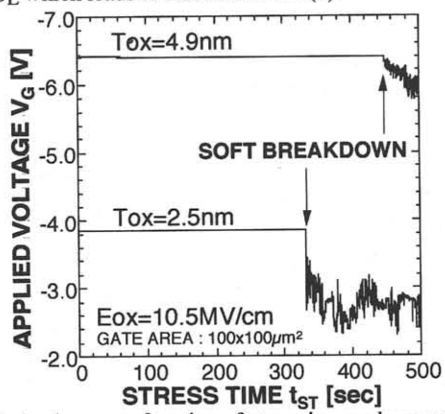

Fig. 6 Applied voltage as a function of stress time under constant current stressing at an identical oxide field at 10.5MV/cm.

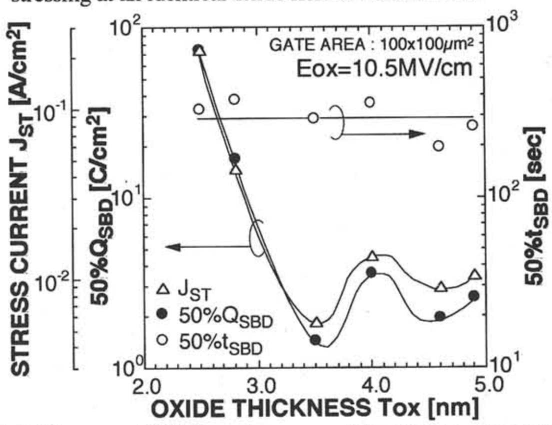

Fig. 7 50%t_{SBD} and 50%Q_{SBD} to cause soft breakdown are plotted as a function of oxide thickness. Also, the stress current J_{ST} at Eox=10.5MV/cm is plotted.

References

[1] K. Okada et al., Ext. Abst. of 1994 Int. Conf. on SSDM (1994) p. 565.
[2] S. H. Lee et al., IEDM Tech. Dig. (1994) p. 605.
[3] T. Yoshida et al., Ext. Abst. of 1996 Int. Conf. on SSDM (1996) p. 539.
[4] M. Depas et al., IEEE Trans. ED **43** (1996) 1499.
[5] B. E. Weir et al., IEDM Tech. Dig. (1997) p. 73.
[6] E. Miranda et al., Appl. Phys. Lett. **73** (1998) 490.
[7] T. Sakura et al., IEDM Tech. Dig. (1998) p. 183.
[8] T. Yoshida et al., Jpn. J. Appl. Phys. **34** (1995) L903.
[9] R. Degraeve et al., IEDM Tech. Dig. (1995) p. 863.
[10] T. Tanamoto and A. Toriumi, Jpn. J. Appl. Phys. **36** (1997) 1439.
[11] D. J. Dimaria and J. H. Stathis, Appl. Phys. Lett. **70** (1997) 2708.
[12] T. Yamazaki et al., MRS. Symp. Proc. **318** (1994) 419.
[13] E. Hasegawa et al., J. Electrochem. Soc. **142**. (1995) 273.
[14] J. W. McPherson and H. C. Mogul, J. Appl. Phys. **84** (1998) 1513.
[15] M. Fukuda et al., Jpn. J. Appl. Phys. **37** (1998) L1534.