Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 324-325

Effects of Hydrogen and Deuterium Annealing on Plasma Process-Induced Damages

C.G. Ahn, J.H. Kim, Y.K. Kim[1], Y.H. Lee[1], and B.K. Kang

Pohang University of Science and Technology, Department of Electrical Engineering,
San 31 Hyoja-Dong, Pohang, Kyungpook, Korea.
Phone: +82-562-279-2226, Fax: +82-562-279-2903, E-mail: bkkang@vision.postech.ac.kr
[1]SAMSUNG Electronics Co. Ltd., Semiconductor Business, ASIC Division,
San24, Nongseo-ri, Kiheung-Eup, Yongin, Kyungki-Do, 449-900, Korea.

1. Introduction

During the plasma processes for ULSI fabrication, the thin gate oxides can be exposed to a high electric field, and the electric field can affect the fixed oxide charge and interface state densities. The interface state density is reduced when the damaged device is annealed in either a H_2 or D_2 ambient [1,2]. Recently, it has been reported that a device annealed in a deuterium ambient is much more tolerant to a stress field than the one annealed in hydrogen ambient [2]. Also, it has been reported that deuterium annealing is more effective at neutralizing the interface states than hydrogen annealing [3]. In this work, the effects of low temperature hydrogen and deuterium annealing on the plasma process induced damage for a device with a gate oxide thickness of 5nm are examined with charge pumping method.

2. Experimental

The substrate material was a p-type (100) CZ silicon wafer with electrical resistivity of 10Ω·cm. The test device with LDD structures were formed using a standard CMOS process. The gate oxide thickness was 5nm, and the effective channel length and width were 0.35μm and 8.75μm respectively. The antenna patterns were a peripheral comb type with a line width of 0.35μm and the antenna ratio (AR) of 1 ~ 10k. These antenna patterns were exposed to plasma only for the poly-Si gate or metal processes. To examine H_2 effects on plasma process induced damages, the test samples were annealed at 450°C for 2 hours in a H_2 (7.5% in N_2) ambient after the metal-1 process. The D_2 annealing effects were examined at 450°C and 480°C for 90min., 2 hours, and 3 hours, respectively. Contrary to the H_2 annealing process, the D_2 annealing treatments were performed after the full process flow. The stability of H_2 and D_2 passivation was observed after applying the ac voltage stress of the pulse waveform to the gate electrode.

3. Results and Discussions

For an n-type MOSFET, the charge pumping currents were measured and the results are shown in Fig. 1. The samples subjected to the poly-Si gate process (poly-Si gate sample) show much less CP currents than those subjected to the metal process (metal sample). The peak CP current is a measure of the interface state density, indicating that the metal process induced more interface states than the poly-Si gate process. The CP current increases with the antenna ratio for metal samples. The effects of H_2 and D_2 annealing on CP current are shown in Fig. 2. D_2 annealing was more effective than H_2 annealing for both the metal and poly-Si gate samples. These results indicate that the D_2 annealing is more effective at reducing interface states than H_2 annealing. When the sample was subjected to H_2 annealing and then to D_2 annealing, the effect of additional H_2 annealing was small. The Si-D bond is more resistant to hot carrier excitation than the Si-H bond. This may be caused by the coupling of the Si-D bending mode with Si bulk phonons resulting in a reduced dissociation rate compared to Si-H. The ac voltage stress tests with the stress pulse height are shown in Fig. 3. In Fig. 3, maximum CP current is abruptly increased at 3.2V of the gate stress voltage. This means that the accelerated electron has the sufficient energy to break bonds if the voltage is higher than 3.2V. Therefore, we applied the gate voltage of 3.2V for the electrical stress tests. The stability of interface property was observed after applying an ac voltage stress and the results are shown in Fig. 4. The CP current increases monotonically with stress time. The rate of increase in CP current is increased with the antenna ratio for both the poly-Si gate sample and the metal sample. This result implies that there is the latent damage, which may be reappeared by the applied stress. The effect of the D_2 annealing temperature and time on stress is examined in Fig. 5. The stability on stress is enhanced at higher annealing temperature. When the H_2 annealing precedes the D_2 annealing, the better stability of the interface properties is shown. However, at 480°C of D_2 annealing temperature, the preceded hydrogen pretreatment has little effect. The stability on the stress for the samples annealed at different annealing ambience is shown in Fig. 6. The D_2 annealing is more effective than H_2 annealing, and the rate of increase of the D_2 annealed sample is almost the same as that of the no annealed sample. The Si-H bond has almost the same bond strength as that of Si-D bond. But the mass of hydrogen is smaller than that of deuterium, and the Si-H bond has a higher vibration frequency than Si-D bond. This in part may gives rise to the large kinetic isotope effect observed under stress conditions [2, 4]. However, the mechanism of D_2 annealing with H_2 pretreatment needs further understanding.

5. Conclusions

For a test device with a gate oxide thickness of 5nm, the metal process induced more plasma damage than the poly-Si gate process. D_2 annealing was very effective in curing the interface damage and enhanced the strength to withstand an electrical stress. When D_2 annealing temperature and/or time increased, or H_2 annealing preceded, the stability is enhanced

significantly. The mechanism of D_2 annealing needs further explanation.

References

[1] H. C. Shin and Cheming Hu, Semicond. Sci. Technol. **11** (1996) p. 463.

[2] J. W. Lyding and K. Hess, and I. C. Kizilyalli, Appl. Phys. Lett. **68** (1996) p. 2526.

[3] S. Krishnan, S. Rangan, S.Hattangady, G. Xing, K. Brennan, M. Rodder, and S. Ashrok, IEDM (1997) p. 445.

[4] K. Hess, I. C. Kizilyalli, J. W. Lyding, IEEE Tr. ED. **45** (1998) p.406.

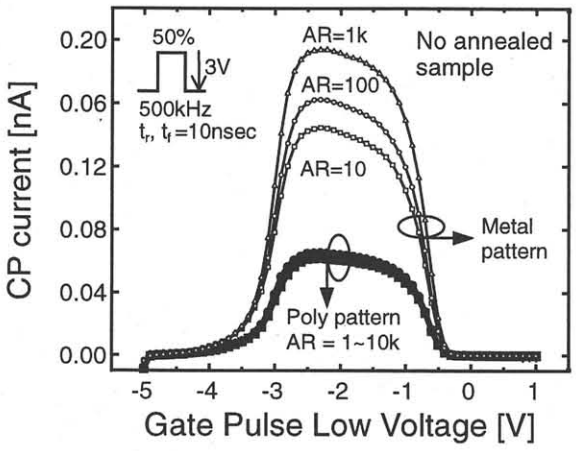

Fig. 1. Charge pumping currents for poly-Si gate and metal samples.

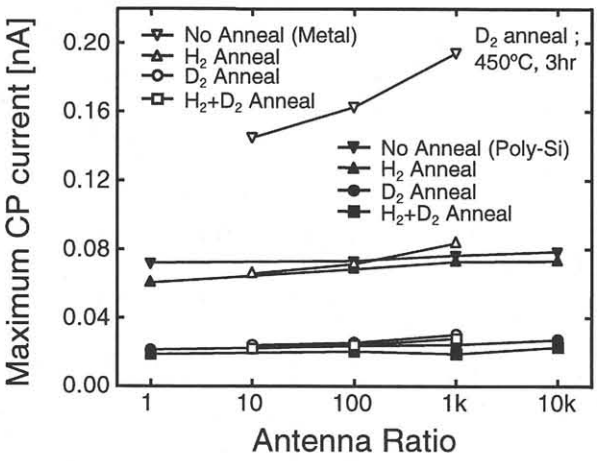

Fig. 2. Maximum CP currents versus antenna ratio for the samples annealed at different annealing ambience.

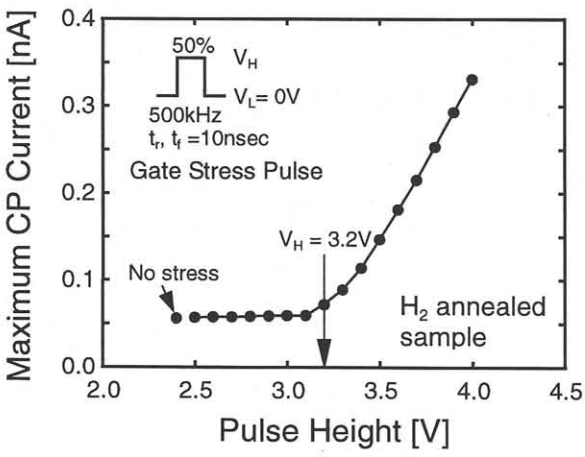

Fig. 3. Maximum CP currents versus the pulse height for the ac pulse stress test.

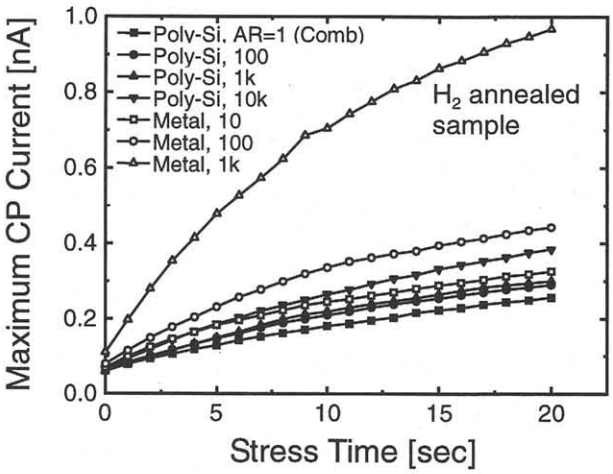

Fig. 4. Maximum CP currents versus the ac stress cycle for poly-Si gate and metal sample. 1 Stress cycle = 1sec

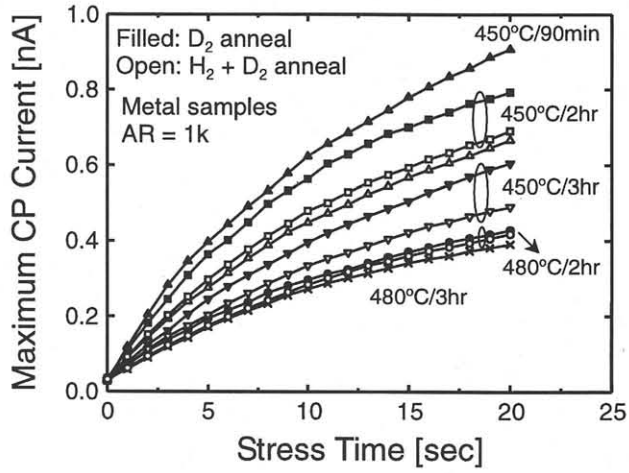

Fig. 5. Dependency of the stability on stress for the Deuterium annealing temperature and time.

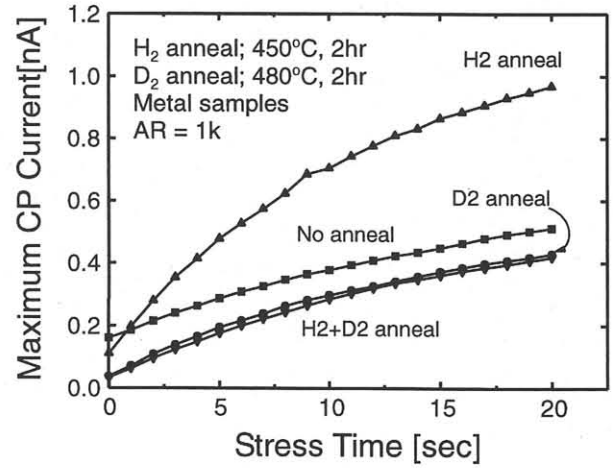

Fig. 6. The stability on the stress for the samples annealed at different annealing ambience