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Influence of Gate Oxide Quality on Plasma Process-Induced Damage in Ultra Thin Gate Oxide

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Introduction

Plasma process-induced charging damage has been a major reliability concern in the manufacturing of MOS devices. This problem becomes worse as the gate oxide thickness is reduced to 3–4nm range. When the gate oxide thickness is further reduced to below 3nm, however, the damage starts to decrease [1], and at around 2nm, the damage becomes negligibly small [2]. These reports suggest that the plasma damage in the advanced scaled-down LSIs with gate oxide thickness of 2–3nm range may not be a big problem. On the contrary, we report here that the plasma damage does not necessarily decrease when the gate oxide becomes thinner. Our study on the plasma damage behavior of MOS devices fabricated using several process sequence suggests that thinner gate oxide becomes more susceptible to the plasma process-induced charging if the rest of the fabrication processes other than the plasma processes are not optimized.

Experimental Procedure

Plasma damage from dielectric etching of contact holes was evaluated using nMOSFET (L/W=0.25μm/10μm) that has multiple contact holes on the gate polysilicon. The number of contact holes is 10, 2.5K and 190K, and referred to as small, medium and large. The gate oxide thickness was 1.9-3.0nm (optical). Three types of gate electrodes were formed using different process sequence (Table 2). They are a stacked polysilicon (thickness: 150nm), a single-layer poly-silicon (thickness: 200nm), and a single-layer poly-silicon (thickness: 150nm), and referred to as process A, B and C. Gate electrode was doped with arsenic implantation at a dose of $2E15cm^{-2}$ at 50keV.

Results and Discussion

Gate oxide thickness dependence of contact etching-induced gate oxide leakage failure in the case of process A is shown in Fig.1. The yield of nMOSFETs improved with a decrease in the gate oxide thickness. At 1.9nm, high yield was observed indicating robustness of thin oxide under plasma charging, consistent with the reported result [1].

However, when other processes were applied for forming the gate electrode (process B and C), we observed oxide degradation (Fig.2) even in the case of 1.9nm oxide. Cumulative probability plot of the gate leakage current also supports this observation (Fig. 3). Thus, superior reliability of ultra thin oxide is not necessarily guaranteed depending on the fabrication process.

In order to investigate the reason for the difference among the process splits (A, B and C), we evaluated the yield of large nMOS capacitors with gate oxide area of $7200\mu m^2$. Since the nMOS capacitor used here has no contact antenna, its yield reflects the base oxide quality free from the plasma damage. As shown in Fig.4, the gate leakage failure of large nMOS capacitors also depended on the gate formation process. Note a good correlation between the yield of large nMOS capacitor and that of nMOSFET with contact antenna shown in Fig. 3. This suggests that the gate formation process affected the base oxide quality, and resulted in enhancing susceptibility of thin (1.9nm) oxide to plasma charging.

This correlation is more clearly shown in Fig.5, which shows the yield of nMOSFET with contact antenna in relation to that of the large MOS capacitor. When the gate oxide thickness was 3.0nm, yield of nMOSFETs with contact antenna is almost constant for each contact antenna size independent of the yield of large MOS capacitors. As the gate oxide thickness is reduced, however, the yield of nMOSFETs with contact antenna started to depend on the yield of large MOS capacitors. Thus, superior reliability of ultra thin oxide under plasma charging diminished due to a decrease in the base oxide quality.

The mechanism of the enhanced plasma damage due to gate electrode formation process is proposed as follows (Fig.6). The three types of gate electrodes have different thickness and grain structures. This difference affects channeling during arsenic implantation [3] or diffusion of arsenic into the gate oxide during a subsequent anneal, and changes the oxide quality by introducing defects. These defects behave as weak paths for injected charges during plasma charging. When the gate oxide is thin (< 3nm), most of the charging current from the plasma flows through the oxide as direct tunneling current, and thus the oxide damage is usually reduced in thin oxide. However, if the oxide has defects and the charging current is too large, current density at the defects becomes high and causes oxide breakdown even when the oxide is as thin as 2nm. Thus, controlling gate oxide quality throughout the fabrication process is important in realizing charging-free MOS devices with ultra thin gate oxide.

Conclusion

With gate oxide scaling below 3nm, plasma-induced charging causes less damage to the oxide only when the oxide quality is well maintained. When the fabrication processes are not optimized, thinner oxide becomes more susceptible to the plasma charging since the rest of the processes can degrade the base reliability of the oxide.

References

[1] S. Krishnan et al., IEDM Tech. Dig., p.601,1998.
[2] K. Noguchi et al., IEDM Tech. Dig., p.441,1997.
[3] H. Ito et al., IEDM Tech. Dig., p.635,1997.

Table 1 : Number of Contacts

Small	: 10
Medium	: 2.5 k
Large	: 190 k

Table 2 : 3 types of gate electrode

Process A	Stacked PolySi 150nm
Process B	Single-layer PolySi 200nm
Process C	Single-layer PolySi 150nm

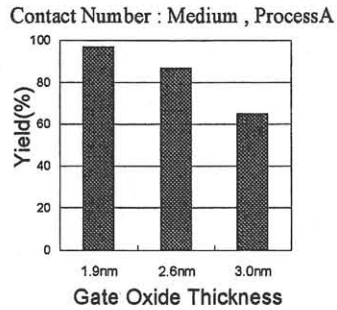

Fig.1 Yields of nMOSFETs for contact antenna devices defined from Ig. As the gate oxide became thinner, the yield improved.

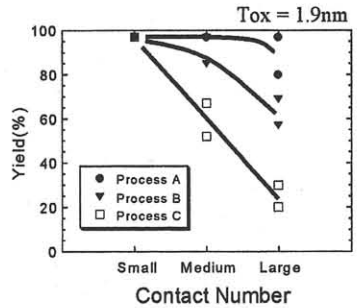

Fig.2 Yields of nMOSFETs as a function of contact number. In process A, the yield did not degrade very much. In process C, the yield degraded as the contact number was increased.

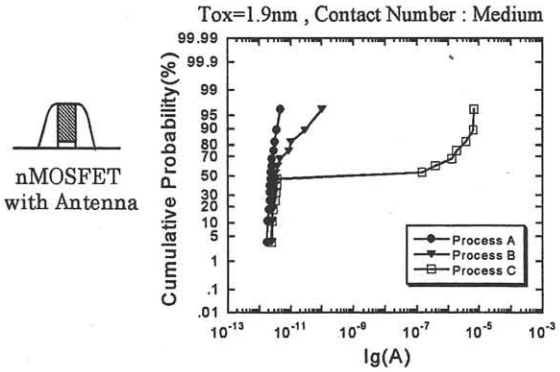

Fig.3 Cumulative probability of Ig for nMOSFET (L/W=0.25μm/10μm) with contact antenna. Ig was measured at Vg = -1V.

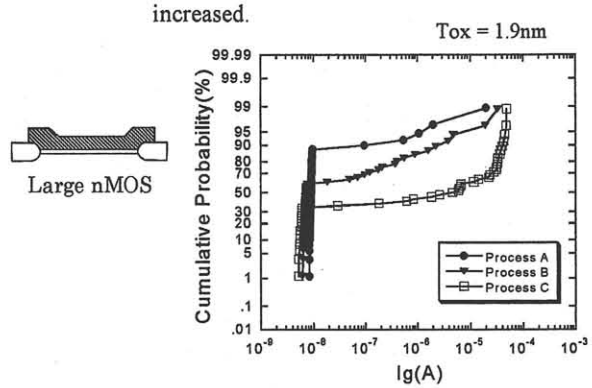

Fig.4 Cumulative probability of gate leakage current (Ig) for large nMOS capacitor with 3 types of gate electrode. The gate oxide area is 7200μm^2. Ig was measured at Vg = -1V.

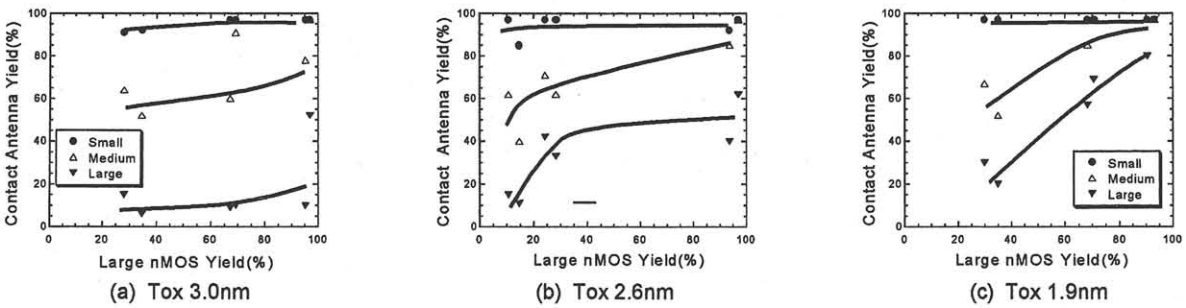

Fig.5 Relationship between the yield of nMOSFETs with contact antenna and that of large nMOS capacitors. In the case of 3.0nm, contact antenna yield was independent of the yield of large nMOS capacitor. As the gate oxide thickness was reduced to 1.9nm, the yield of nMOSFETs with contact antenna showed a clear dependence on the yield of large nMOS capacitors, which reflects base oxide quality.

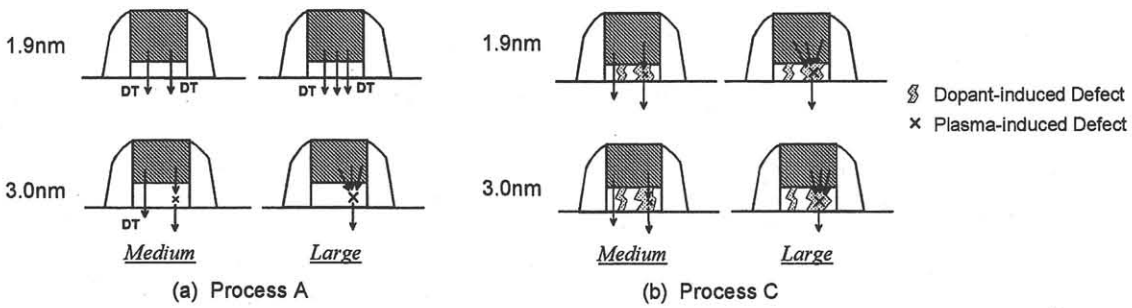

Fig.6 Schematic diagram of the proposed oxide breakdown model. Dopant-induced oxide defects were created during the gate electrode formation. When the charging current is large, current density at the defects becomes high and causes oxide breakdown even when the gate oxide is very thin.