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MOS Characteristics of NH_3-Nitrided N_2O-Annealed Oxides Fabricated at Reduced Pressure

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1. INTRODUCTION

Ultrathin gate oxides for deep-submicron MOS devices have become a major concern mainly due to hot carrier effects [1,2] and boron penetration [3]. Nitrided oxides have been proposed as a promising alternative gate dielectric to the conventional oxides. Many nitrided oxides have been prepared mostly in atmospheric pressure using NH_3 or N_2O. However, from the manufacturing point of view, it is highly desirable to develop processes that do not deviate significantly from the conventional processes to retain process simplicity. In this paper, a new technique, namely NH_3-nitrided N_2O-annealed oxides (NNO) fabricated at reduced pressure vertical furnace, is presented to attain the desired nitrogen concentrations and profiles that eventually improve the hot-carrier lifetime and high immunity to boron penetration. The NNO dielectrics fabricated at reduced pressure (<550 torr) showed excellent hot-carrier lifetimes and barrier property to boron penetration without any other adverse effects on electrical properties and reliability.

2. DEVICE FABRICATION

N-MOSFETs (NMOS) and P-MOSFETs (PMOS) with various gate dielectrics were fabricated. LOCOS isolation and threshold voltage (V_{th}) adjustments were performed. After removal of thin sacrificial oxides, various gate dielectrics (Table.1) were fabricated at different process condition. N_2O-oxides and NNO dielectrics were fabricated by annealing SiO_2 in reduced pressure NH_3 and/or N_2O. Wafers with various gate dielectrics were processed together through poly-Si deposition. After patterning and reoxidation of poly-Si gate, shallow S/D extensions called MDD [1] were made with BF_2 and As. After sidewall spacer patterning, poly-Si gates and S/D regions were heavily doped with BF_2 for PMOS and with As for NMOS. These implants were activated by RTA. $CoSi_2$ salicide process was performed for reduction of gate electrode and S/D resistance.

3. RESULTS AND DISCUSSION

SIMS depth profilings were performed on several nitrided samples. Unlike N_2O-oxides with only one nitrogen peak at bottom interface, NNO dielectrics have two nitrogen peaks at both top and bottom interfaces (Fig.1). Nitrogen atoms at top interface are likely to be incorporated during NH_3-nitridation. Even though the peak nitrogen atoms at bottom interface may play an important role in preventing boron penetration, for even thinner oxides, however, they alone may not completely prevent boron penetration. This strongly implies a potential benefit of NNO dielectrics for that. Drain current (I_{DS}) and transconductance (G_m) were plotted as a function of gate voltage (V_{GS}) in Fig.2. For NMOS devices, NNO and N_2O-oxides show lower peak G_m at low-field than that of conventional oxide, but they have higher peak G_m at high-field (Fig.2-(a)). For PMOS devices, no significant difference in peak G_m is observed (Fig.2-(b)). Hot carrier lifetimes were extracted fron NMOS devices with 55 Å gate dielectrics. Lifetimes of NNO gate dielectrics were ~7x longer than those of conventional oxides (Fig.3). Unlike conventional oxides, NNO dielectrics exhibited no significant shift in V_{th} (Fig.4), implying their high immunity to boron penetration. For TZDB characteristics investigated, NNO dielectrics showed at least comparable distribution to conventional oxides, indicating that NNO dielectrics fabricated at reduced pressure may have no significant NH_3-nitridation induced microdefects.

4. CONCLUSION

A new technique, namely NH_3-nitrided N_2O-annealed oxide (NNO) formation, is proposed and demonstrated to obtain the desired nitrogen concentration and profiles. This technique could improve hot-carrier lifetime and resistance to boron penetration in ultrathin gate dielectrics. This technique may have a great impact on deep-submicron CMOS technology.

RFERENCES

[1] B. S. Doyle et al., IEEE Electron Device Lett., **14**, pp.536 (1993)
[2] K. Mistry et al., IEEE Electron Dev. Lett., **12**, pp.492 (1991)
[3] J. M. Sung et al., IEDM Tech. Dig. pp.447 (1989)

[Table1] Oxide charge (Q_{ox}), interface state density (D_{it}), oxide thickness (T_{ox}), peak nitrogen concentration ([N]), interface roughness (Ra) for 55Å gate dielectrics

Sample Name	Q_{ox} (q/cm^2)	$D_{it}(cm^{-2}.eV^{-1})$	T_{ox}	[N] (atomic%)	Ra (nm)
Conventional Oxide	9.6E10	6.7E10	55Å	~0	0.135
N_2O-Oxide	2.0E11	1.1E11	55Å	1.1	0.136
NNO-1	2.8E11	9.3E10	57Å	2.6	-
NNO-2	3.1E11	1.0E11	56Å	3.2	0.144

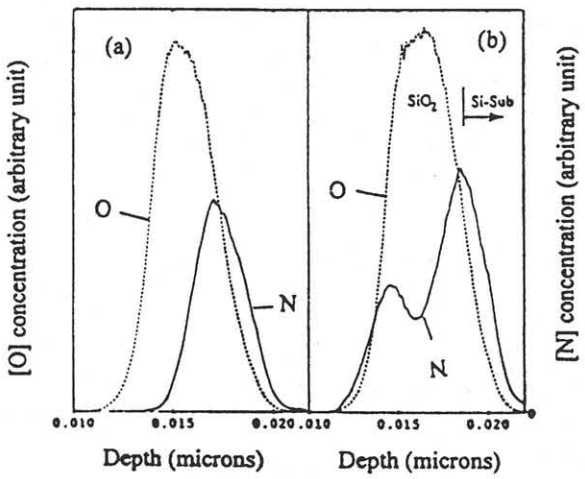

Fig.1 SIMS depth profiles for 85Å nitrided gate dielectrics: (a) N_2O-Oxide and (b) NNO samples

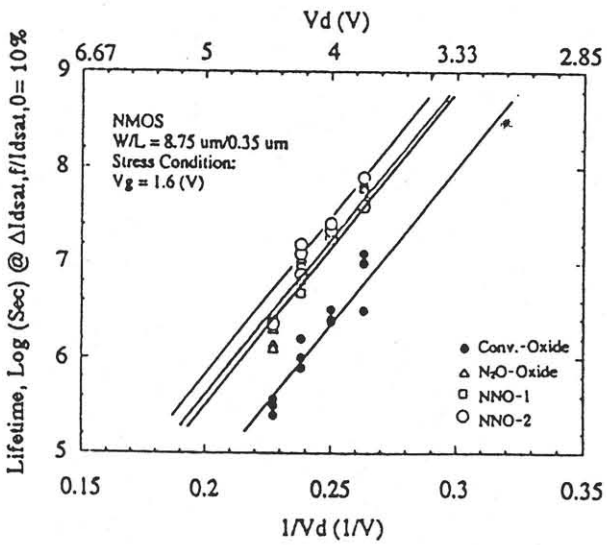

Fig.3. Extracted lifetimes of NMOS devices with 55 Å different gate dielectrics

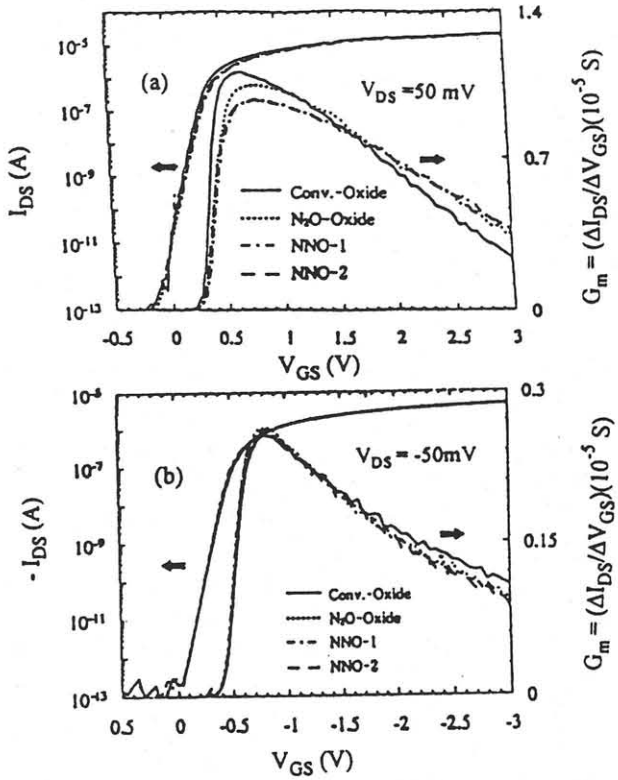

Fig.2. Drain current and transconductance characteristics for 55Å gate dielectrics: (a) NMOS and (b) PMOS devices (W/L = 40μm/40μm)

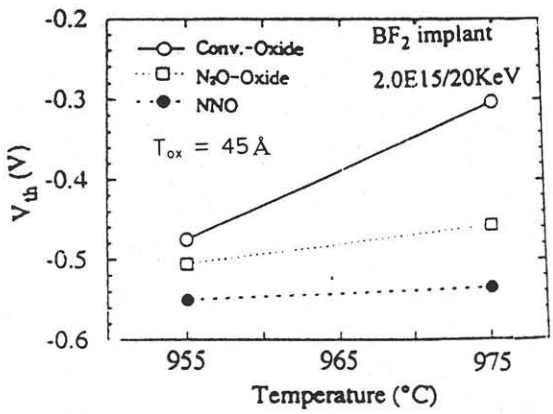

Fig.4. Shift in threshold voltage of PMOS devices