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# Novel Ultra Thin Heavily Nitrided Gate Dielectrics Technology Adding Fluorine for Highly Reliable MOSFETs

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## Introduction

Below 3nm ultra thin gate dielectrics boron penetration is crucial issue and nitridation process is indispensable.[1] It is reported that the nitridation process makes traps in gate dielectrics especially in nitridation using NH3. Therefore post oxidation is necessary for those nitrided gate dielectrics. However that oxidation process makes the effective dielectric thickness thick.[2] In this paper we present the new technology adding fluorine to heavily nitrided ultra thin gate dielectric. Moreover electric properties of MOSFET with this new gate dielectric are discussed.

## Experiments

In this experiment we used the standard dual gate CMOS process. Gate dielectrics were formed after the isolation formation. At first silicon surface was oxidized with N2O, then nitrided process was carried out in NH3 atmosphere. Both processes were carried out in conventional furnace process at 900 ℃. After gate poly-Si deposition, fluorine was implanted into the poly-Si gate with low implantation energy. After source-drain implantation, The activation anneal was executed at 900℃ for 10 minutes. Implanted fluorine diffused into the gate dielectric during this annealing process. Gate dielectric formation process was summarized in Fig.1. Film thickness in this experiment denotes the initial N2O oxidized thickness which were measured by the ellipsometry.

## Results and Discussion

*A. Nitrogen concentration*

Fig.2 shows the XPS spectra of N1s. Each initial N2O oxidation film thickness was 2.5nm. By N2O oxidation 0.5 % nitrogen concentration was detected in gate dielectric. On the other hand after NH3 nitridation 9.0% nitrogen was incorporated into gate dielectric. Therefore much nitrogen was incorporated into ultra thin gate dielectric using NH3 nitridation.

*B. Device characteristics*

Fig.3 shows C-V characteristics of nitrided and non nitrided ultra thin gate dielectrics. Each initial film thickness was 2.5nm. Nitrided gate dielectric had about 10% larger capacitance. This phenomenon was due to higher dielectric constant of nitrided gate dielectrics. Besides, no change of the gate dielectric capacitance was observed in the adding 5e14/cm$^2$ fluorine doses sample. From these large capacitance, nitrided device have the advantage of high drive current.

Fig.4 shows Ig-Vg characteristics for NMOS. The lowest gate leakage current was obtained in the fluorine implanted sample at a low voltage range. We expect that the decrease of leakage current is due to the decrease of trapping sites of fluorinated gate dielectrics.

Fig.5 shows PMOS Ig-Vd characteristics using NH3 nitrided and non nitrided gate dielectric. Initial film thickness was 2nm. In the case of fluorine implanted non nitrided gate dielectric sample, strong boron penetration was observed. On the contrary, adding the NH3 nitridation sample, boron penetration was successfully suppressed even in the fluorine implanted gate dielectric. The flat band voltage shift was below 50mV in 2nm thickness gate dielectric even with the condition of 1e15/cm$^2$ fluorine implanted doses.

Fig.6 shows PMOS subthreshold slope versus the amount of doses of fluorine using the NH3 nitridation dielectrics process. Until fluorine doses reach 5e14/cm$^2$, the subthreshold slopes were smaller than that of non fluorine dosed samples and subthreshold slope began to deteriorate above that value of fluorine doses, finally the subthreshold slopes with fluorine doses of 1e15/cm$^2$ became larger than that of non fluorine doped sample. This tendency is universal in each gate dielectric thickness. These results indicated that the fluorine improves the interface between the Si substrate and gate dielectric, in the fluorine doses below 5e14/cm$^2$.

Fig.7 and 8 show transconductances for NMOS and PMOS. In both cases, peak Gm value was improved about 10 % by nitridation. Moreover peak Gm value was improved by fluorine implantation. We expect that these results originated in the excellent interface of fluorinated gate dielectrics.

Fig.9 and Fig.10 show subsreshold characteristics and Id-Vd characteristics for NMOS and PMOS adding fluorine to nitrided ultra thin gate dielectrics with a 0.18um gate length. The nominal drive currents are 600uA/um for NMOS and 320uA/um for PMOS at 1.8V operation. We have achieved a low off current value of 20pA/um for NMOS and 5pA/um for PMOS while maintaining high drive current.

*C. Reliability characteristics*

Fig.11 shows the results of hot-carrier reliability experiments. The experiments were carried out under maximum substrate current condition. The early stage of degradation was largest in non nitrided dielectric. However the degradation rate of nitrided gate dielectric was the fastest. It is reported that nitridation by NH3 brings hydrogen in gate dielectric, and make traps in gate dielectrics.[2] Those trap sites were expected to originate from weak Si-H bonds (3.18eV). By adding fluorine to gate dielectrics smallest degradation was achieved in all region. This result expected to originate from changing Si-H bonds to stable Si-F bonds (5.73eV) in gate dielectric.[3] Fig.12 shows the proposed mechanism of fluorine in ultra thin gate dielectric. In non fluorinated gate dielectric there are dangring bonds and weak Si-H bonds. Therefore such bonds cause interface deterioration and rapid degradation of transistor property. On the other hand in fluorinated gate dielectric, diffused fluorine atoms terminate dangring bonds and change weak Si-H bonds into stable Si-F bonds. As a result, excellent interface and highly reliable gate dielectric was successfully achieved.

## Summary and Conclusion

A new technology for achieving ultra thin gate dielectrics was demonstrated. We clarified that the adequate amount of fluorine makes the Si-gate dielectric interface improve in heavily nitrided gate dielectric film. No boron penetration, small subthreshold slope, high tranceconductance and longer hot-carrier lifetime were obtained in N- and P-MOSFET with 2.5nm heavily nitrided gate dielectric adding fluorine. This new technology is very effective for ultra thin gate dielectric, which is used less than 0.18um MOSFETs.

## References

[1]B.Maiti et al.,IEDM Technical Digest, p651 (1997)
[2]T.Hori et al.,IEEE Electron Devices, 36, p340 (1989)
[3]P.Chowdhury et al., Appl Phys.Lett. 70(1) p37 (1997)

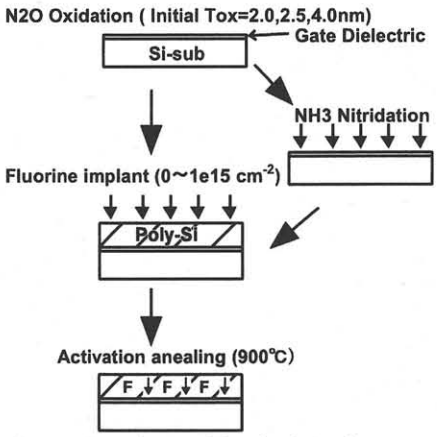


Fig.1 procedure of gate dielectrics formation

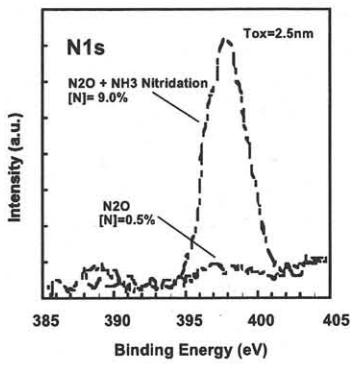


Fig.2 XPS spectra of N1s

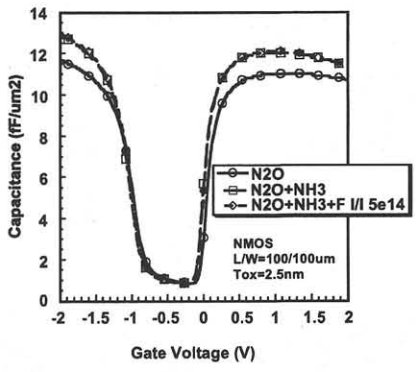


Fig.3 C-V characteristics

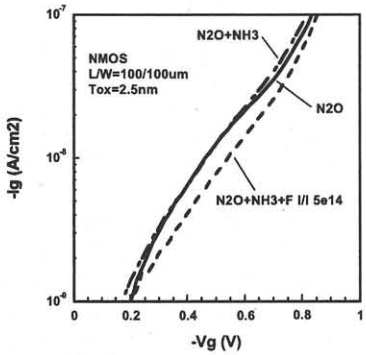


Fig.4 Ig-Vg characteristics of NMOS

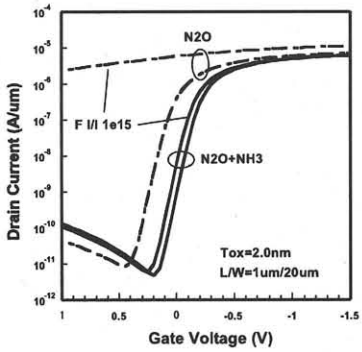


Fig.5 Id-Vg characteristics of PMOS

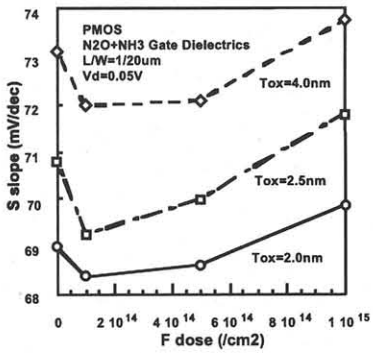


Fig.6 Fluorine dose dependence of S-slope

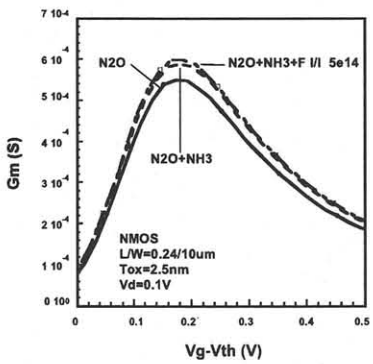


Fig.7 Gm vs (Vg-Vth) characteristics of NMOS

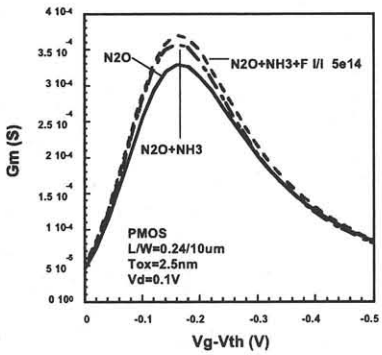


Fig.8 Gm vs (Vg-Vth) characteristics of PMOS

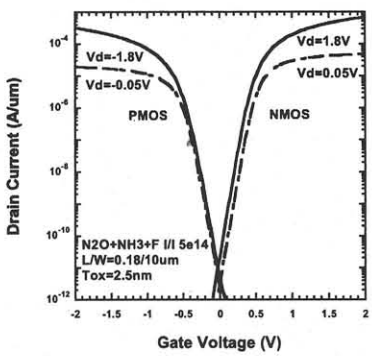


Fig.9 Subsreshold characteristics

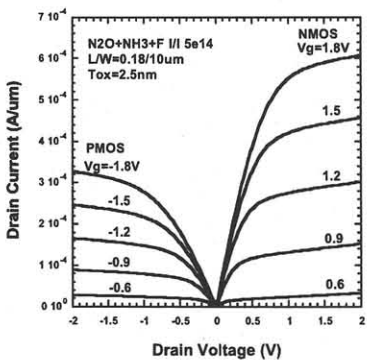


Fig.10 Id-Vd characteristics

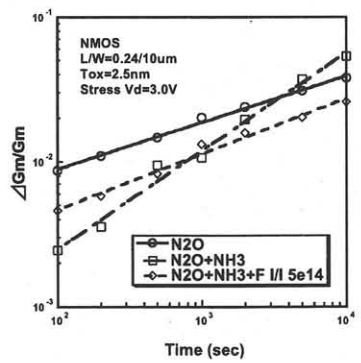


Fig.11 Time dependence of Gm degradation in NMOS

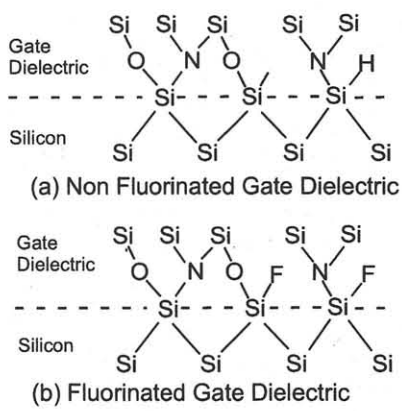


Fig.12 Proposed mechanism of fluorine
(a) Non Fluorinated Gate Dielectric
(b) Fluorinated Gate Dielectric