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Latent Damage Generation in Submicrometer MOS Devices Under High-Field Impulse Stressing and Its Characterization Using Flicker Noise Measurement

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1. Introduction

Decreasing feature sizes in submicrometer MOS device technologies have resulted in a deterioration of the oxide-breakdown protection margin (difference between the junction breakdown trigger voltage and oxide breakdown voltage) under electrostatic discharge (ESD) or high-field impulse stress. The use of epi-CMOS can also raise the trigger voltages of silicon controlled rectifiers used in ESD protection circuits to levels higher than the oxide breakdown voltage. There will also be situations when the oxide does not break down catastrophically under low-level ESD transients but may suffer sufficient latent damage to impact the long-term reliability of the device [1]. Although the types and distribution of traps generated under constant current or constant voltage stress have been studied extensively, such information on damages created under short-duration, high-field impulsive stress are not widely available.

2. Experimental Details

The p-channel MOS capacitors used have phosphorus-doped polycide gates and gate areas ranging from 33,300 to 50,000 μm^2 (8 nm and 13 nm thick oxides) and 50,000 to 200,000 μm^2 (14.7 nm thick oxides). The transistor devices used for the subthreshold and noise measurements are 0.35 μm technology LDD nMOSFETs with 7 nm oxide thickness. The nMOSFETs have a gate width of 50 μm and mask gate lengths of 0.25, 0.35 and 0.5 μm. The high-field impulse stressing of the gate oxides was performed using a single-pulsing transmission line technique [2] by applying 6 to 25 high voltage pulses of 200 ns duration to the gate electrode of the pMOS capacitors (stress pulse magnitude = 26 V for an oxide field of 20 MV/cm and a current density of 130 A/cm^2) and the nMOSFETs (stress pulse magnitude = 12 -15 V). The source, drain and substrate terminals of the nMOSFETs were grounded during the high-field impulse stressing.

3. Results and Discussion

Figure 1 shows there is hardly any difference in the charge-to-breakdown (Q_{bd}) values of the two groups of ESD-stressed devices as compared to the virgin devices, despite the fact that latent damage, in the form of trapped holes and neutral electron traps as determined from C-V measurements, are present in the ESD-stressed devices [2]. The purpose of the constant voltage stress CVS step (performed at an oxide field of 9.6 MV/cm for 50 s) is to electrically anneal the trapped holes and to fill up the neutral electron traps created during the ESD stress [3]. The high-field impulse stressing was also carried out on nMOSFETs which were then subjected to a subsequent hot-carrier stress step under maximum substrate current ($I_{sub(max)}$) conditions at a drain voltage (V_d) of 4 V and a gate voltage (V_g) of 1.55 V to investigate the effect of the ESD pre-stress on the subsequent hot-carrier reliability. Figure 2 shows the amount of interface traps (δN_{it}) and oxide trapped charges (δN_{ot}) generated during the $I_{sub(max)}$ stress, as determined using McWhorter's method [3]. Devices which have been subjected to a high-field ESD pre-stress have slightly greater amounts of interface states generated during the subsequent $I_{sub(max)}$ stress. The ESD-stressed devices also suffer from greater electron trapping, which is larger than the interface trap generation, during the hot-carrier stress. The results indicate that high-field impulse stressing lead to latent damages within the device which could result in increased trap generation during the subsequent hot-carrier stress. Figure 3 shows that there is linear relationship between δN_{it} (and also δN_{ot}) and $|\delta G_{m(max)}/G_{m(max)}|$. The multitude of trap formation and filling somehow complicate the detection of ESD latent damage as it is difficult to set a criterion for latent damage based on the densities of the extracted traps. An alternative is to monitor the $G_{m(max)}$ degradation with ESD stress, as $\delta G_{m(max)}$ encompasses the combined effect of the generated interface states and bulk traps. However, the change in $G_{m(max)}$ may not be sufficiently sensitive for monitoring small levels of latent damage induced by the high-field ESD stress, especially in thin-oxide devices.

Figure 4 shows that the input referred noise power (S_{Vg}) increases as the maximum transconductance $G_{m(max)}$ decreases for the 0.25 μm, 0.35 μm and 0.5 μm gate length nMOSFET devices. It has been reported that interface traps and border oxide traps generate flicker noise in accordance with the McWhorter's carrier number fluctuation theory and/or the Hooge's mobility fluctuation mechanism. The unified flicker noise model proposed by Hung *et al.* [4] incorporates both the number and surface mobility fluctuation mechanisms as

$$S_{Vg} = \frac{kTq^2}{\gamma f WLC_{ox}^2}(1+\alpha\mu N)^2 N_t(E_{fn}), \qquad (1)$$

where k, T, q, γ, f, W, L, C_{ox}, α, μ, N_t *and* E_{fn} are the Boltzmann constant, temperature, electronic charge, attenuation coefficient of the oxide electron wave function, measurement frequency, gate width, gate length, oxide capacitance per unit area, coulombic scattering coefficient, carrier mobility, oxide trap density and quasi-fermi level of electrons respectively. The measurement of S_{Vg} is performed at a constant constant effective gate voltage (V_g - V_{th}) = 0.6 V in Fig. 4 so as to minimise the bias dependency of S_{Vg} as the threshold voltage V_{th} of the device changes with stressing. It is seen from Fig. 4 that S_{Vg} has a power-law relation to $1/G_{m(max)}$ which can be expressed as

$$S_{Vg} = A\left[\frac{1}{G_{m((\max)}}\right]^B, \qquad (2)$$

where A and B are constants which can be obtained from the fitted straight line to the measured data points in Fig. 4. It was found that B ranges from 2.4 to 6 while that of A ranges from 2.1×10^{-27} to 5.9×10^{-19} for devices from this 0.35 μm process technology. Since B is larger than unity, it implies that the characterization of the latent damage arising from high-field ESD stressing can be performed more sensitively using low-frequency noise measurements as compared to monitoring the degradation in the maximum transconductance. The amount of ESD-stress generated traps δN_t was also obtained from flicker noise measurements using (1) by assuming that the carrier number fluctuation mechanism is the dominant mode of flicker noise generation. The results, using $1/\gamma = 2\times10^8$ cm^{-1}, are shown in Fig. 5. It is seen that the trap densities $\delta N_{t(eff)}$, estimated from flicker noise data, and slope of the plot are comparable to those calculated using McWhorter's method.

4. Conclusion

Latent damage in thin oxides, caused by high-field impulse stressing, has a significant impact on the subsequent trap generation within the device under hot-carrier stressing but not on the charge-to-breakdown distribution. Characterization of such latent damage can be carried out more sensitively using low-frequency noise measurements.

References

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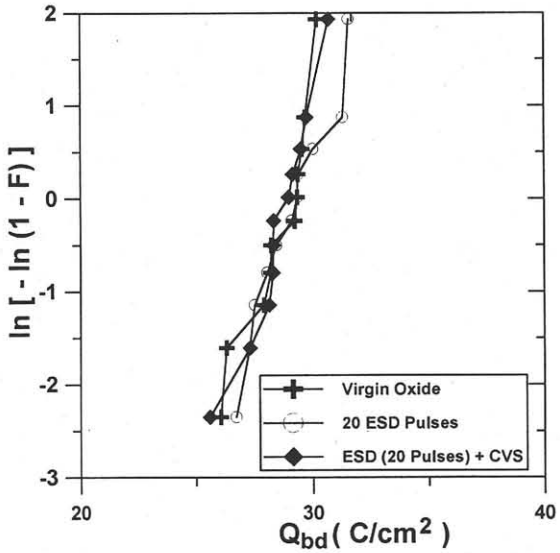

Figure 1: Weibull plot showing Q_{bd} distribution of p-MOS capacitors. The Q_{bd} measurements were performed at a current density of 1.5 mA/cm^2, with 11 devices in each of the 3 groups (total of 33 devices used).

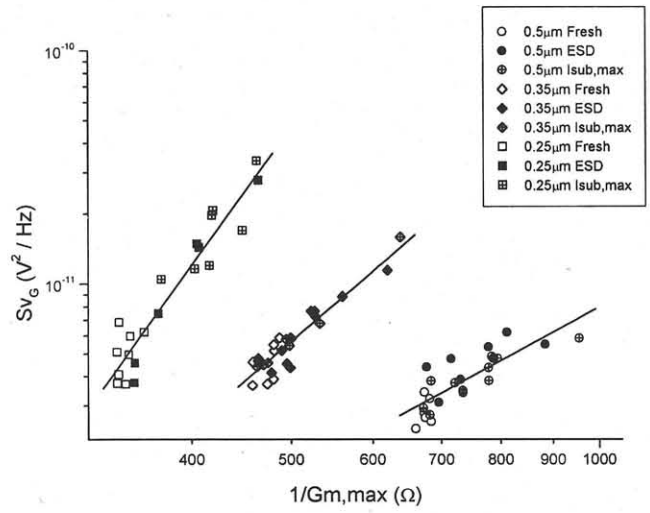

Figure 4: The relationship between input referred noise power S_{Vg} and $1/G_{m(max)}$ for the fresh or virgin nMOSFET devices (indicated by crosses), devices subjected to varying degrees of the ESD pre-stress (indicated by triangles), and the ESD pre-stressed devices after hot-carrier stressing under $I_{sub(max)}$ conditions (indicated by circles). The solid lines represent the best fit straight lines to the measured data points for the 0.25 μm (square symbol), 0.35 μm (diamond symbol) and 0.5 μm (circle symbol) gate length nMOSFET devices.

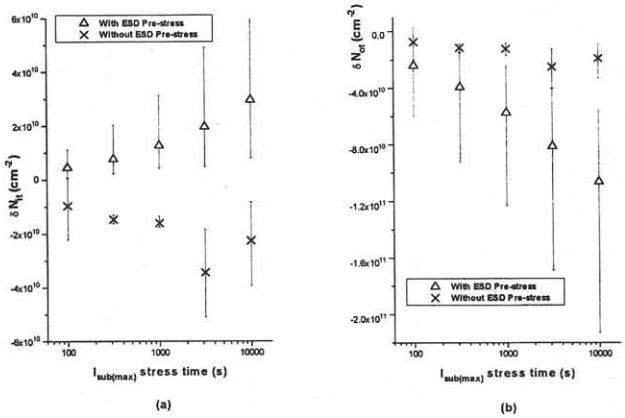

Figure 2: Number of (a) interface traps (δN_{it}) and (b) oxide trapped charges (δN_{ot}) generated during the maximum substrate current ($I_{sub(max)}$) hot-carrier stressing for 0.35 μm gate length nMOSFETs (gate width = 50 μm) without the ESD pre-stress (indicated by crosses) and devices which have been subjected to varying degrees of high-field impulse stressing (indicated by triangles) to simulate different amounts of latent damage as a result of the ESD pre-stress. The line bar at each stress time represents the minimum, maximum and average values of the measurements performed on 4 devices. In (a), a positive (negative) δN_{it} value means that the subthreshold slope of the device becomes larger (smaller) after stress. In (b), a negative δN_{ot} value implies electron trapping.

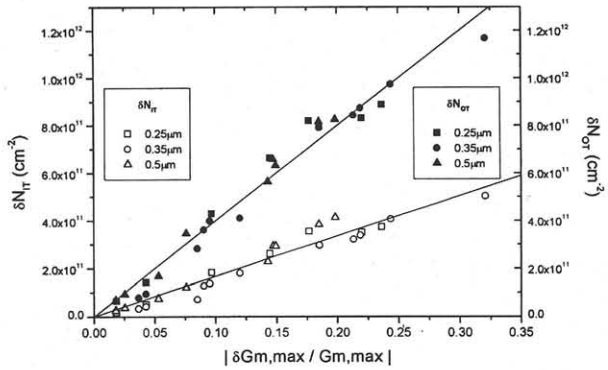

Figure 3: The amount of interface traps (δN_{it}) (solid circles) and oxide trapped charges (δN_{ot}) (open circles) generated during the ESD pre-stress versus the absolute fractional change in the maximum transconductance ($|\delta G_{m(max)}/G_{m(max)}|$) for the nMOSFET devices with mask gate lengths of 0.25 μm, 0.35 μm and 0.5 μm. The maximum transconductance was measured at a drain voltage of 0.1 V.

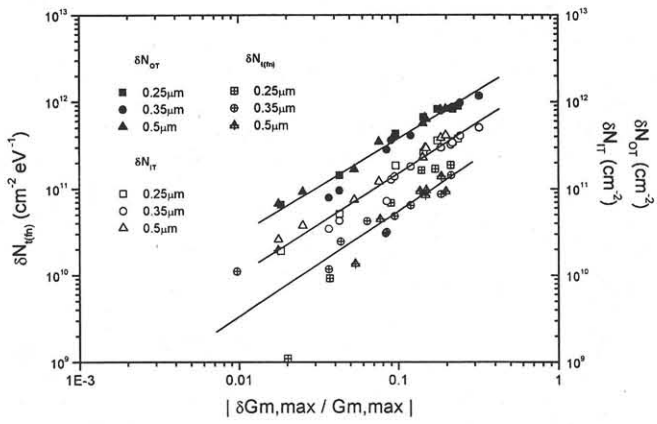

Figure 5: Change in the trap density $\delta N_{t(eff)}$ at the quasi-Fermi level, calculated from flicker noise measurements at a frequency of 10 Hz, compared with the change in interface state and trapped charge densities (δN_{IT} and δN_{OT}) determined using McWhorter's method [3]. The nMOSFET devices, with gate lengths of 0.25 μm, 0.35 μm and 0.5 μm, were subjected to varying degrees of ESD stress.