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Invited

(Ba, Sr)TiO_3 Stacked Capacitor Technology for 0.13μm-DRAMs and Beyond

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1. Introduction

(Ba,Sr)TiO_3 (BST) is a promising candidate for capacitor dielectrics of dynamic random access memories (DRAMs) in 0.10 - 0.13 μ m generations[1-5]. The issues to be solved for application of BST in DRAM cell capacitors are chemical vapor deposition (CVD) of BST, electrode technology, electrode connection to plug, protection against backend process damage, and BST capacitor reliability, as shown in Fig.1.

In this paper, two issues among them, i.e. electrodes technology and CVD of BST film , are discussed.

2. Electrode technology

Electrode material selection is important, because electrical characteristics of BST capacitor are strongly affected by electrode material. We proposed All PErovskite Capacitor (APEC) technology [5], in which $SrRuO_3$ (SRO) was used as both storage node and plate electrodes. Comparing with BST capacitors with Pt and Ru electrodes, APEC has several advantages, as shown in table 1. The patterning of SRO by dry etching is thought to be difficult. However, we considered that both storage node and plate SRO electrodes could be patterned by chemical mechanical polishing (CMP) and wet etching, respectively.

Although both Pt and Ru electrodes have poor adhesion on SiO_2, peeling or blistering of SRO film did not occur during BST deposition on SRO electrode.

SRO/BST/SRO capacitors showed lower leakage current than Ru/BST/Ru capacitors. SRO is an oxide material. Moreover, the crystal structure of SRO is perovskite structure as same as BST and the lattice parameter of SRO is very close to that of BST. So, less oxygen vacancies and smoothness due to lattice continuity at SRO/BST interface attribute to the lower leakage current in SRO/BST/SRO capacitors.

Figure 2 shows the change of leakage current by DC stressing for both SRO/BST/SRO and Ru/BST/Ru capacitors. The leakage current increase of SRO/BST/SRO capacitors is less than that of Ru/BST/Ru capacitors, indicating that SRO/BST/SRO capacitors had higher reliability compared with Ru/BST/Ru capacitors. The higher reliability of SRO/BST/SRO capacitors is considered to be due to metal-oxide electrode, which acts as a sink for oxygen vacancies.

The H_2 anneal resistance was also improved drastically by using SRO electrode because SRO does not have the catalytic effect as in Pt and Ru electrode.

3. BST CVD technology

The requirements for BST CVD are good step coverage and good electrical characteristics (low leakage current and high permittivity). Step coverage and electrical properties of CVD BST films depend on deposition temperature, as shown in Table 2. There is trade-off relation between electrical properties and step coverage. CVD under kinetically limited condition is essential to obtain good step coverage.

We proposed In-situ Multi-Step (IMS) CVD[6], which is a sequential repetition of low temperature (~400 ℃) deposition of ultra thin BST film (<10nm) and high temperature crystallization (~650 ℃) in one chamber as shown in Fig.3. For IMS-CVD, we used a hot-wall batch-type CVD equipment with high heating (100℃/min.) and cooling (50℃/min.) rates.

Figure 4 shows a step coverage of BST deposited by IMS-CVD on the concave (hole) storage node structure. The step coverage was >80%.

Figure 5 shows a leakage current of the SRO/BST/SRO capacitor. The leakage current density was $<10^{-7}$ A/cm^2, which was one order of magnitude lower than the case of single step BST deposition at 400℃. One of the reason of the low leakage current in IMS-CVD BST is due to the lower residual carbon concentration in IMS-CVD BST than that of single-step CVD BST, as shown in Fig.6.

The SiO_2 equivalent thickness (t_{eq}) of 37nm-thick BST was 0.43nm, corresponding to 330 of permittivity. Figure 7 shows a cross sectional TEM dark field image of BST deposited on concave structure. BST on SRO electrode is twinkling but BST on SiO_2 film is not, indicating that the crystallinity of BST on SRO is better than that on SiO_2. Thus, high permittivity is obtained by using SRO electrode.

4. Summary

We proposed APEC technology for electrode and IMS technology for BST CVD. By introducing the both technologies, we achieved BST capacitors with low leakage current, high permittivity, and good step coverage. These

technologies are promising for 0.13 μ m stacked DRAM and beyond. The remained issues to be solved are CVD technology of SRO electrode and barrier metal development between storage node SRO and a metal plug.

References

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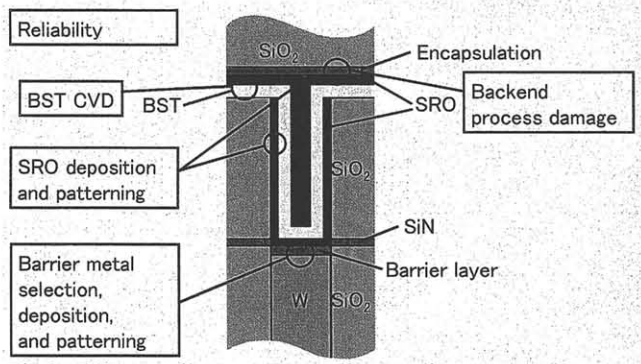

Fig.1 BST capacitor structure and process issues.

Table 1 Comparison of electrode material

	Pt	Ru	SRO
Work function	5.6 – 5.7 eV	4.5 – 4.7 eV	-
Resistivity	10 μ Ω cm	12 μ Ω cm	600 μ Ω cm
Adhesion	Poor	Poor	Good
Leakage current	Good	Good	Better
Reliability	Poor	Poor	Good
H_2 anneal resistance	Poor	Poor	Better
Dry Etching	Possible	Easy	Difficult
CMP	-	Possible	Possible
Wet etching	Difficult	Difficult	Easy

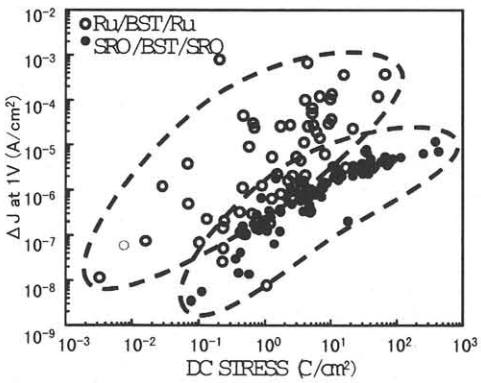

Fig.2 Leakage current change by DC stress.

Table 2 Comparison of low and high temperature CVD of BST

Deposition temperature	Low temperature (~400℃)	High temperature (>500℃)
Step coverage	Good	Poor
Permittivity	Low (~200)	High(~350)
Leakage current	High	Low

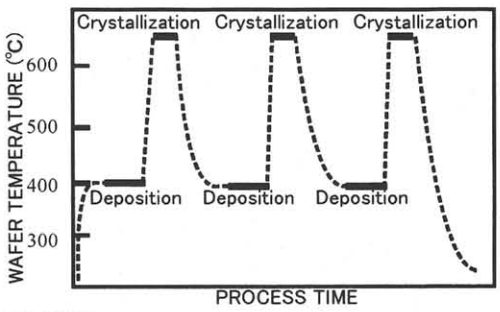

Fig.3 IMS-CVD process.

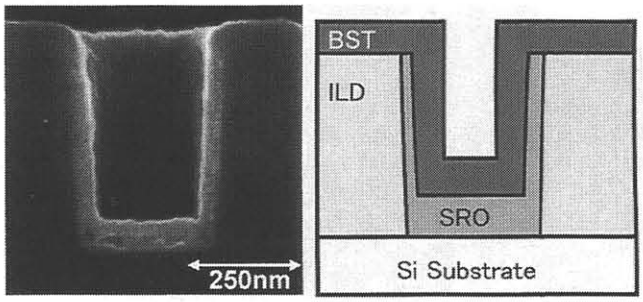

Fig.4 Step coverage of BST deposited by IMS-CVD.

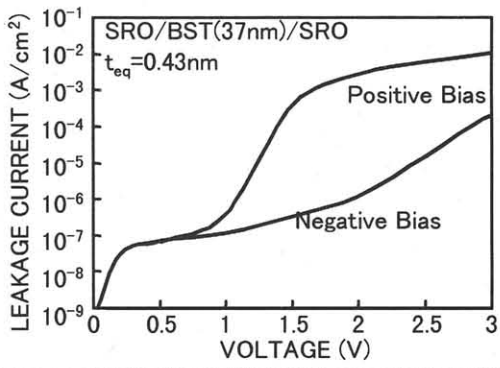

Fig.5 Leakage current of SRO/BST/SRO capacitor by IMS-CVD.

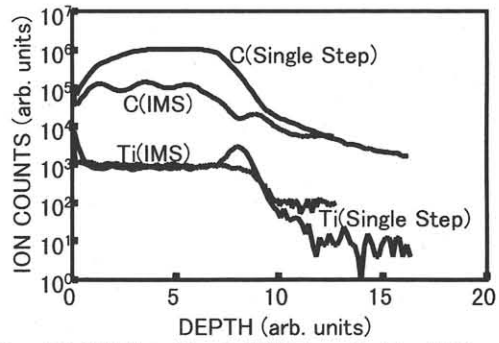

Fig.6 C and Ti SIMS profiles in BST deposited by IMS and single-step CVD.

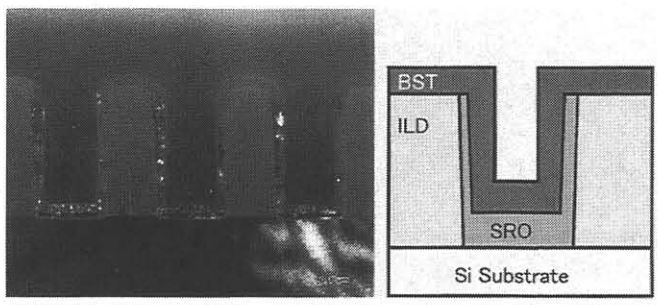

Fig.7 TEM dark field image of BST.