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Low Temperature Recovery of $Ru/(Ba, Sr)TiO_3/Ru$ Capacitors Degraded by Forming Gas Annealing

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1. Introduction

$Ru/(Ba,Sr)TiO_3$(BST)/Ru capacitors using the BST films deposited by ECR plasma CVD at an extremely low temperature below 250 °C has been developed [1]. For the application of the BST capacitors to DRAMs, degradation by forming gas (H_2+N_2) annealing (FGA) [2] is still an issue. The degraded properties of the capacitors should be recovered by low temperature process in inert ambient to avoid desorption of hydrogen from dangling bonds in the depletion layers which leads to degradation of MOSFETs and oxidation of wiring.

In this paper, a low temperature N_2 post-annealing of the Ru/BST/Ru capacitors at below 400 °C is proposed (Fig.1). The electrical properties of the capacitors are completely recovered by this post-annealing to the initial level applicable to Gbit-scale DRAMs without affecting the MOSFETs characteristics.

2. Experimental

BST thin films were deposited on Ru bottom electrodes by ECR plasma CVD at 200 °C. Detailed BST deposition conditions are shown in Table I. After annealing the BST films by RTA at 700 °C in N_2 ambient, 50 nm-thick Ru top electrodes of 0.07 mm^2 were formed by dc sputtering at room temperature. These capacitors were annealed in N_2 for 40 min at 400 °C.

The FGA was performed in 5%-H_2/95%-N_2 at 300 to 400 °C for 40 min. After the FGA, post-annealing was carried out in N_2 or O_2 at 300 to 450 °C for 20 to 60 min. The capacitors before and after the FGA were evaluated by XRD and SIMS. The effect of N_2 post-annealing on the electrical properties of the MOSFETs and the junction leakage current was also investigated.

3.Results and Discussion

Recovery of Leakage Current by Post-annealing

The endurance of the Ru/BST/Ru capacitors to the FGA depends on the temperature of the FGA. The leakage current of the capacitors almost remains unchanged after the FGA at up to 300 °C. On the other hand, in the case of 400 °C-FGA, the leakage current drastically increases after the FGA, as shown in Fig.2. The N_2 post-annealing even at the low temperature of 300 °C improves the leakage current characteristics degraded by the FGA to the initial level of the as-fabricated capacitors (Fig.2). As shown in Fig.3, the leakage current increased by the FGA decreases with N_2 post-annealing time and recovers to the initial level by annealing for more than 40min while t_{eq} of 0.51 nm before the FGA is not influenced by both the FGA and the N_2 post-annealing.

The effect of the post-annealing performed in O_2 ambient as well as N_2 ambient on the leakage current is shown in Fig.4. The leakage current decreases with more than 4 orders by both N_2 and O_2 post-annealing at 300 °C. Figure 5 shows the change of the leakage current when a capacitor is annealed in the forming gas and in N_2, alternately. Reversible changes of the leakage current occur by annealing in the forming gas and in N_2. From the results shown in Figs. 4 and 5, it is suggested that the thermal energy given by the post-annealing is the cause of the recovery.

No change in the composition of BST films after the FGA is observed in the SIMS measurement. Even the hydrogen content remains unchanged after the FGA, as shown in Fig.6. The XRD diffraction yields of BST also remains unchanged after the FGA.

According to the results described above, the mechanism of the leakage current change by the FGA and the post-annealing may be as follows; small amount of hydrogen, hardly detectable by SIMS measurement, induce defects which enhance the leakage current. These defects can be diminished easily by the low temperature post-annealing.

The temperature of post-annealing required to improve the leakage current characteristics is much lower than that of previous report [2]. This is probably because the BST films in this study are deposited at the extremely low temperature and consist of granular-like structure grains [1] different from columnar structure grains observed in the BST films deposited at higher temperature.

Applicability of N_2 Post-annealing to ULSI Processes

Figure 7 shows the leakage current of N^+P junction annealed in the forming gas and subsequently annealed in N_2 at various temperatures. The leakage current remains unchanged before and after the N_2 post-annealing carried out at less than 400 °C because hydrogen atoms terminating the Si dangling bonds are stable below 400 °C [3]. Subthreshold characteristics of MOSFETs are also measured after each annealing. No difference in the threshold voltage and the subthreshold slope is observed up to 450 °C. These results indicate that the N_2 post-annealing at 300 °C for the recovery of the Ru/BST/Ru capacitors does not affect the junction leakage current and the MOSFETs characteristics.

The leakage current less than $1.0\times10^{-6}A/cm^2$ at $\pm$ 1.0V is obtained up to 125 °C for the Ru/BST/Ru capacitors after the N_2 post-annealing, as shown in Fig.8. This value is sufficient for Gbit-scale DRAMs and even for the embedded DRAMs for high temperature use.

4.Conclusions

A low temperature N_2 post-annealing process is proposed to recover the electrical properties of Ru/BST/Ru capacitors degraded by forming gas annealing. By using the N_2 post-annealing at 300 °C, the capacitor properties degraded by the FGA is completely recovered to the initial level of t_{eq} = 0.51 nm and $J_L < 1.0\times10^{-7}A/cm^2$ at $\pm$ 1.0V sufficient for Gbit-scale DRAMs without affecting the MOSFETs properties and the junction leakage current. This post-annealing process enables the Ru/BST/Ru capacitors to be suitable to Gbit-scale DRAMs.

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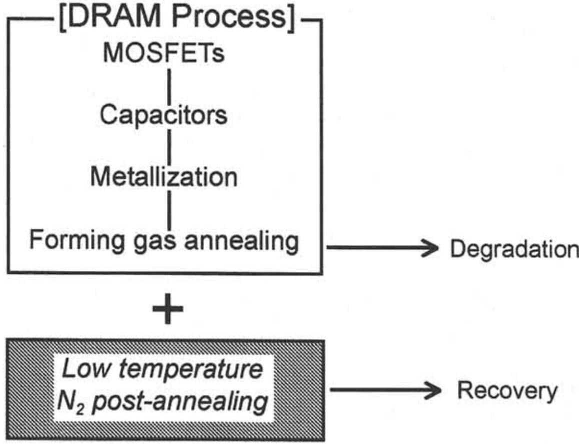

Fig.1 DRAM process sequence and proposed N_2 post-annealing process. The effects on the BST capacitors are indicated with arrows.

Table I BST deposition conditions

Total pressure	4 mTorr
μ-wave power	500 W
Substrate temperature	200 °C
Thickness	18.0 - 19.0 nm
Composition (Ba+Sr)/Ti and Ba/(Ba+Sr)	1.20 and 0.45
Sources	$Ba(DPM)_2$, $Sr(DPM)_2$ and $Ti(O\text{-}i\text{-}C_3H_7)_4$
Substrate	Ru(100 nm)/TiN(50 nm)/Ti(30 nm)/SiO_2(400 nm)/Si

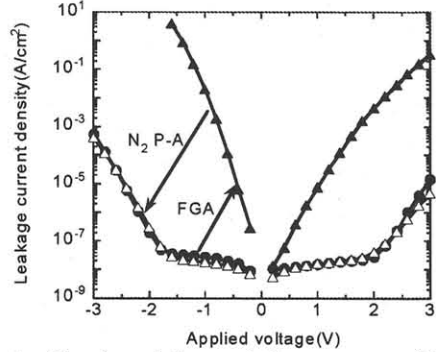

Fig.2 The degradation and the recovery of leakage current characteristics for Ru/BST/Ru capacitors by forming gas annealing (FGA) and N_2 post-annealing (P-A), respectively. (●; as fabricated, ▲; forming gas annealed at 400 °C and △; N_2 post-annealed at 300 °C for 40 min, respectively.)

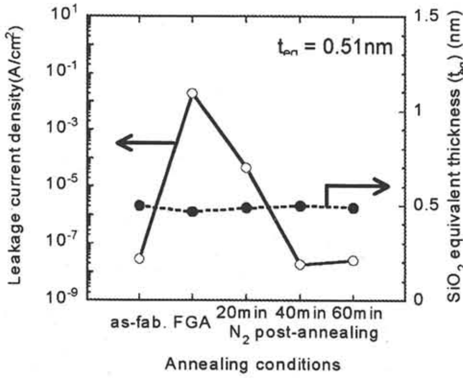

Fig.3 Dependence of leakage current at -1.0V and t_{eq} on the duration time of N_2 post-annealing. The FGA and the N_2 post-annealing were carried out at 400 °C and 300 °C, respectively.

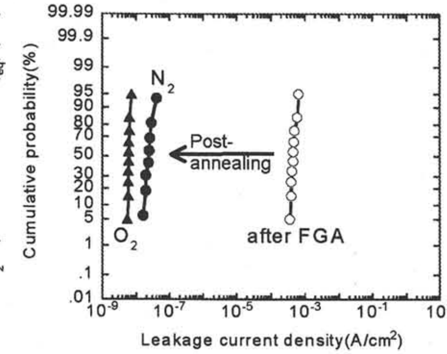

Fig.4 Dependence of leakage current density at -1.0V on post-annealing atmosphere at 300°C. The FGA was performed at 400 °C for 40 min.

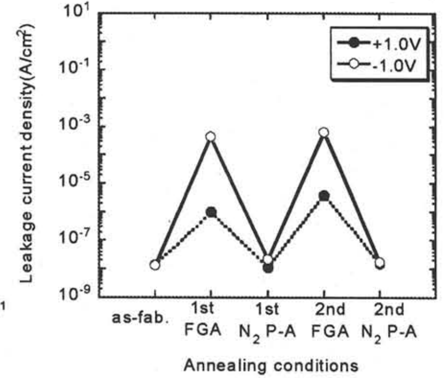

Fig.5 Leakage current density after successive annealing in forming gas and in N_2. The P-A indicates post-annealing carried out at 400 °C for 40 min. The FGA was performed at 400 °C for 40 min.

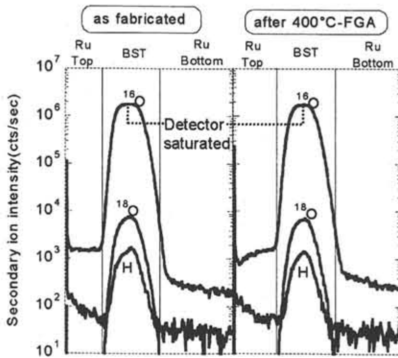

Fig.6 Oxygen and hydrogen depth profiles in BST films analyzed by Secondary Ion Mass Spectroscopy.

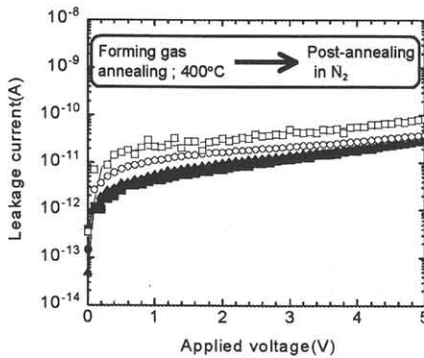

Fig.7 Dependence of N^+P junction leakage current on the N_2 post-annealing temperature. The FGA was performed at 400 °C for 40 min. (●; after the FGA, ■, ▲,○ and □; post-annealed in N_2 at 200, 300, 400 and 450 °C, respectively.)

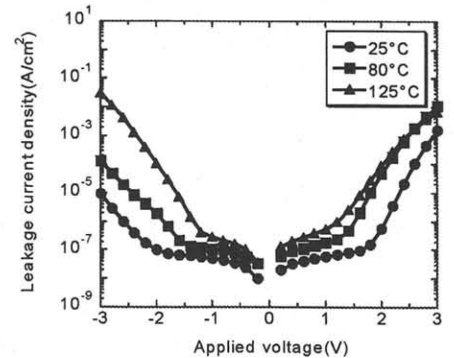

Fig.8 Leakage current characteristics for N_2 post-annealed capacitors measured at 25°C to 125°C. The post-annealing was carried out at 300°C for 40min in N_2.