Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 488–489

A-15-3

Enhanced Recovery from Back-End Process Damage by Conductive Perovskite Electrode for BST Capacitor

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1. Introduction

$(Ba,Sr)TiO_3$ (BST) has received much attention as a new dielectric material for 0.13μm DRAM generation and beyond [1-3]. Recently, it is reported that all perovskite capacitor technology with conductive perovskite-oxide electrodes ($SrRuO_3$ (SRO)) can reduce the leakage current and the damage from hydrogen-annealing [4,5]. Considering the DRAM integration, these capacitors would suffer damage from back-end processes such as ILD deposition and via-hole RIE, and it is important to investigate the details of the damage and the means of recovery from it.

In this paper, degradation of all-perovskite BST capacitors during back-end processes and effect of recovery annealing have been investigated. We found the enhancement of recovery by conductive perovskite electrodes containing plenty of oxygen intrinsically. It was clarified that all-perovskite capacitor is a promising candidate for future DRAMs.

2. Experimental

Plane all-perovskite capacitor modules were fabricated on n+doped 8" silicon substrates by sputtering. BST film was prepared at about 400℃ in Ar/O_2 gas mixtures using a ceramic target with the Ba/Sr ratio of 1/1, and annealed for crystallization at 650℃ for 30min in nitrogen. Both top and bottom electrodes were 50nm-thick SRO deposited in Ar atmosphere at 500℃. Top electrodes were formed by lithography and wet etching technique, and we obtained the samples referred to as "Reference".

Some of the samples went to the back-end processes, containing plasma SiO_2 deposition at 400℃ and pad-opening RIE. We call these samples "Damaged". Schematic explanation of the samples and their process flow is shown in Fig.1. Several recovery annealing were tested using these damaged samples under atmospheric pressure, varying the annealing temperature and the ambient gases.

Electrical properties were evaluated at $100 \times 100\mu m^2$-area capacitors with BST thickness of 40nm. The leakage current characteristics were measured by HP4156A semiconductor parameter analyzer system. The capacitance measurements were carried out using HP4284A LCR meter at 1kHz.

3. Results and Discussion

Leakage current characteristics of the samples before recovery annealing is shown in Fig.2. This wafer-level measurement reveals obvious degradation of the sample "Damaged", meaning that the capacitor suffered damage during the back-end processes such as plasma SiO_2 deposition and RIE. Especially, remarkable degradation can be seen in the negatively-biased side, implying that the damage due to plasma processes attacked much more severely the interface of top-electrode and BST. As for the capacitance, almost no change was detected.

Temperature dependence of recovery annealing was investigated. In Fig.3, we can clearly see the degradation of the damaged sample: Schottky current component (steeply increasing with the applied voltage) has greatly increased by the back-end process damage, while relaxation current component (almost constant below 1×10^{-8} A/cm^2) shows only a slight increase. After annealed for five minutes in nitrogen, increased Schottky current have got suppressed. The sample annealed at 600℃ shows better characteristics than the one annealed at 500℃, indicating that it is desirable for the damaged capacitor to be annealed at higher temperature. The leakage current density of the sample annealed at 600℃ is less than 1×10^{-8} A/cm^2 for the range of 3.4V, while its capacitance corresponds to the SiO_2-equivalent thickness of 0.50nm.

To investigate the effect of ambient gases for recovery annealing, two gases, nitrogen and oxygen, were tested. Some of the damaged samples were annealed at 500℃ and 600℃ under atmospheric pressure for five minutes. Results are shown in Fig.4, and there is no obvious difference between two gases. On the other hand, it is reported that the leakage current of Pt/BST/Pt capacitors (without back-end processes) can be decreased only by post-annealed in oxygen, while annealing in reducing ambience causes degradation [6].

The damage-recovery mechanism of our samples could be explained as follows: Back-end processes attack the electrode/dielectric interface and cause some defects such as oxygen vacancies as shown in Fig.5, schematically. For the recovery, it is necessary to compensate the vacancies, and existence of oxygen near the interface is indispensable. From this point, conductive perovskite-oxide electrodes, containing plenty of oxygen intrinsically, can supply oxygen to the damaged interface automatically and enhance the recovery. Just by thermal annealing, all-perovskite capacitor can be recovered from the back-end process damage.

4. Conclusion

We have shown the remarkable degradation of leakage characteristics under negative bias, implying that the damage due to back-end processes attacked much more severely the interface of the top-electrode and BST. This damage can be effectively recovered by annealed at around 600℃, and the leakage current density is less than 1×10^{-8} A/cm^2 for the range of 3.4V, low enough again for DRAM application. Though existence of oxygen is considered to be indispensable for the recovery mechanism, SRO/BST/SRO capacitor can be recovered just by thermally annealing process, due to the oxygen intrinsically contained within the electrodes. This recovery enhancement by conductive perovskite electrodes also enables the annealing process to be inserted anywhere needed in the back-end processes of DRAM fabrication, whether the capacitors are exposed to oxygen ambience or sealed up. All-perovskite capacitor could be a promising candidate for future DRAMs, with the great freedom of back-end integration.

Acknowledgment

Authors would like to thank A.Kojima, R.Nakata, M.Sato, H.Tomita and N.Fukushima for their contribution to this work and helpful discussions. We would also like to thank J.Matsunaga and K.Maeguchi for their encouragement.

References

1) R.B.Khamankar, *et al.*: IEDM 1997 Technical Digest, pp.245
2) B.T.Lee, *et al.*: IEDM 1997 Technical Digest, pp.249
3) Y.Kohyama, *et al.*: Symp. on VLSI Tech. Dig., pp.17, 1997
4) M.Izuha, *et al.*: Jpn. J. Appl. Phys. **36** (1997) pp.5866
5) K.Hieda, *et al.*: IEDM 1998 Technical Digest, pp.807
6) J-H.Joo, *et al.*: Appl. Phys. Lett. **70** (1997) pp.3053

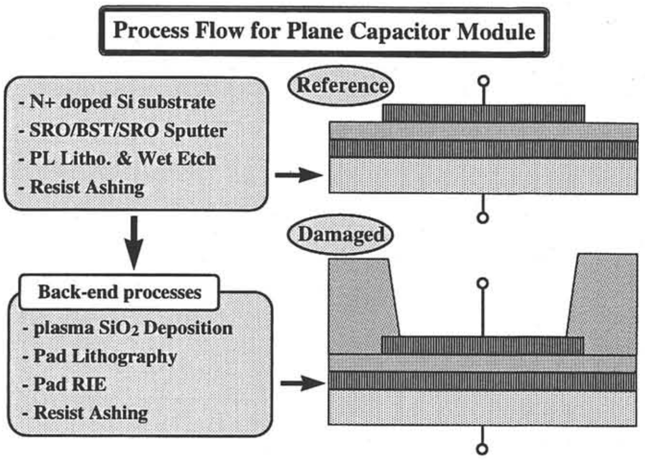

Fig. 1 Process flow for plane capacitor module of the samples used in this experiments. Two samples were prepared: "Damaged" with back-end process damage and "Reference" without damage.

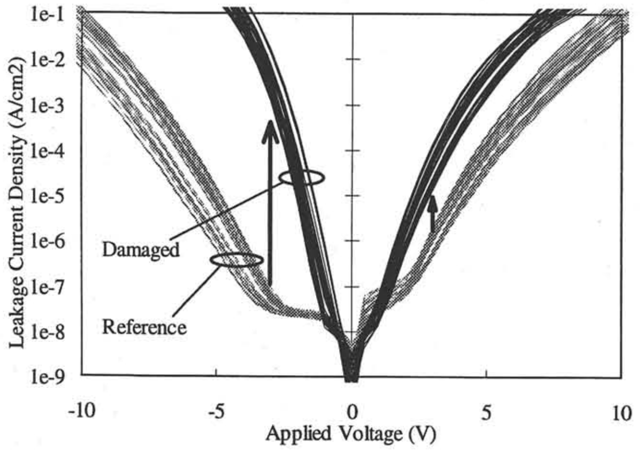

Fig. 2 Wafer-level results of the samples with and without the damage. Vertical axis shows the leakage current density, and horizontal axis shows the bias voltage applied to the top electrode. Remarkable degradation can be seen in the negatively-biased side.

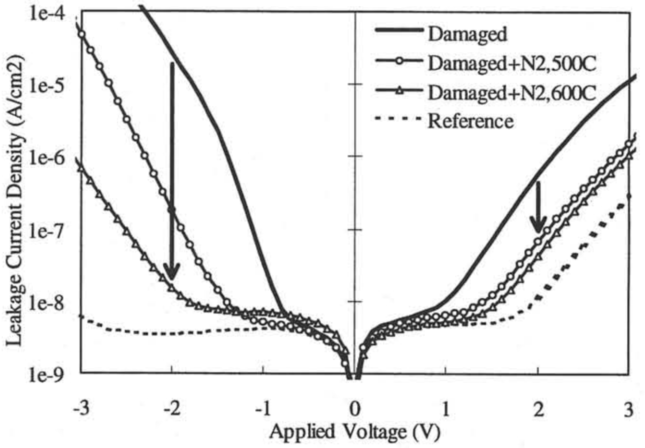

Fig. 3 *J-V* characteristics of the samples "Damaged" annealed at 500℃, 600℃ and before recovery annealing. Annealing was carried out in nitrogen ambience for five minutes. *J-V* curve of the reference sample is also plotted.

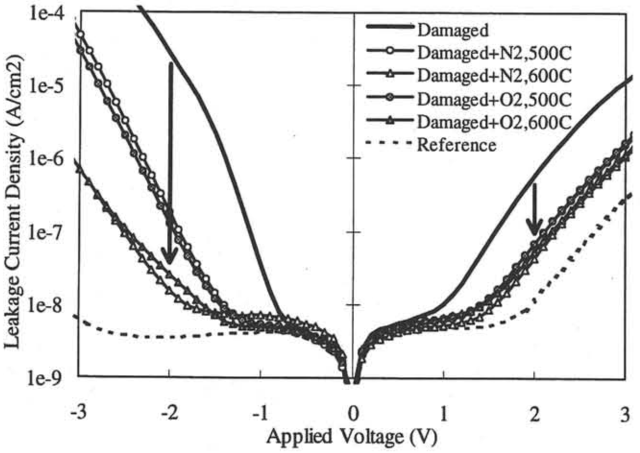

Fig. 4 *J-V* characteristics of the samples annealed in nitrogen and oxygen ambiences. Annealing was performed under atmospheric pressure for five minutes. No obvious difference between two gases can be seen.

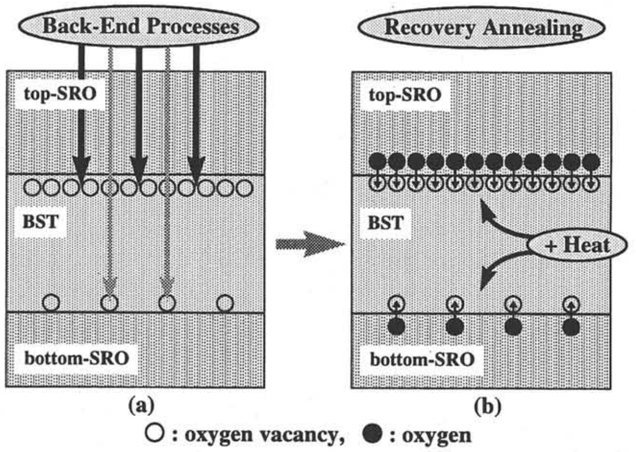

Fig. 5 Schematics of damage and recovery of all-perovskite BST capacitor: (a)Back-end processes attack the SRO/BST interface and cause defects such as oxygen vacancies. (b)After annealing, the damage is recovered by oxygen compensation from perovskite electrodes containing plenty of oxygen intrinsically.