Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 492–493

Ru-Ta_2O_5MIM Capacitor toward 0.1 μm DRAM Cell

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1. Introduction

High-k capacitor technology has extensively studied toward 0.1 μm node device including BST and Ta_2O_5 metal-insulator-metal (MIM) structure [1-5]. Regarding the Ta_2O_5 MIM structure, it has clear advantage to the perovskite dielectric materials in the technology continuity from the Ta_2O_5 metal-insulator-semiconductor (MIS) structure. The possibility of the technology extendibility has been demonstrated up to 0.13 μm node DRAM with the high aspect ratio Ru pillar technology [2]. However the lower dielectric leakage should be required for the thin dielectric used in smaller node as well as the suppression of its temperature dependence. In this study, we discuss the further extendibility of the Ta_2O_5 -MIM technology that can suppress the leakage and its temperature dependence. As shown in Fig. 1, the electrode height in the Ta_2O_5-MIM cylinder structure is comparable to the BST stack structure at 0.13 μm and 0.10 μm. The possibility of the Ru cylinder formation is also discussed.

2. Experiments

Bottom electrode pretreatment is one of the key processes to modify the leakage properties and the temperature dependence since the interface between Ta_2O_5 and bottom electrode is one of the important factors. Micro-roughness and interlayer alike RuO_X at the interface could contribute to the electrical properties.

We compared the two different anneal conditions for the Ru bottom electrodes, one was annealed in Ar, the other in Ar-4%H_2 at 800 °C for 2 minutes. The bottom Ru electrodes were deposited at 450 °C with the conventional RF sputtering in Ar ambient on SiO_2/Si substrates. Then, they were annealed in Ar or Ar/H_2 for stabilization of the bottom electrode prior to the Ta_2O_5 CVD process using $Ta(OC_2H_5)_5$ and oxygen. The Ru grain grew by about 5 times in size and was oriented to <00h> axis. The thickness of the as-deposited Ta_2O_5 film was optically measured to be 17 nm. Post deposition annealing was performed in UV-O_3 ambient. The Ta_2O_5 film was crystallized by rapid thermal anneal at 750 °C in N_2. The top Ru electrode was sputtered through the shadow mask for at room temperature. After the all film deposition, they were annealed at 600 °C to recover the sputtering damages. In the structures of Ru / Ta_2O_5 / Ru, current vs. voltage (I-V), capacitance vs. voltage (C-V) and current vs. time (I-t) characteristics were evaluated.

3. Results and Discussion

The I-V characteristics measured at room temperature slightly depend on the bottom Ru electrode anneal conditions as shown in Fig. 2. The equivalent thickness (T_{eq}) of 0.9 nm was obtained for both samples. However, the temperature dependence of the leakage was affected by the bottom electrode anneal conditions. Figure 3 shows the Arrenius plot of the leakage current at +1V top electrode bias. The difference of the activation energy for them suggested the conduction mechanism could depend on the bottom interface, which might be modified by the different bottom electrode anneal conditions. The time dependence of the leakage current also suggested the change of the mechanism as shown in Fig. 4.

We found that the morphology of the Ru surface was different between the sample annealed in Ar and that annealed in Ar/H_2. Figure 5 shows the Ru surfaces after anneal in each ambient. The difference in morphology could be explained that the residual oxygen in Ar oxidizes the Ru surface during the anneal process. In the Ar annealing process, RuO_x which is volatile could vaporize and the energy minimum (00h) surface of hexagonal Ru crystal could be appeared as shown in Fig. 5 (b). In the Ar/H_2 anneal, the step-and-terrace structure of the grain surface could be formed during the Ru grain growth to minimize the surface energy without the vaporization of RuO_x as in the Ar anneal process. Although more details need to be studied, we believe that difference of the Ru surfaces is one of the major reasons why the temperature dependence of leakage was improved by the bottom electrode annealed in Ar/H_2.

We successfully fabricated the 20nm thick Ru cylinder array structure with the height of 0.3 μm suited for 0.16 μm rule as shown in Fig.6. Figure 7 shows 0.1 μm rule Ta_2O_5-MIM capacitor structure with 25 fF each supposed from our results. The electrical and structural properties can meet the requirements such as low leakage current (~ 0.2fA / cell), low height (~ 0.6 μm), and enough spacing (80nm). The thin Ru formation indicates the possibility of the 0.1 μm DRAM cell with Ru/ Ta_2O_5/Ru cylinder.

4. Conclusions.

We found the method for decreasing the leakage in Ru/ Ta_2O_5 / Ru capacitor by Ar/H_2 anneal of the bottom Ru electrode. The Ru surface annealed in Ar/H_2 ambient had the step-and-terrace structure. We also demonstrated the Ru /Ta_2O_5 /Ru crown structure, which could be used for 0.1 μm rule DRAM cell.

References

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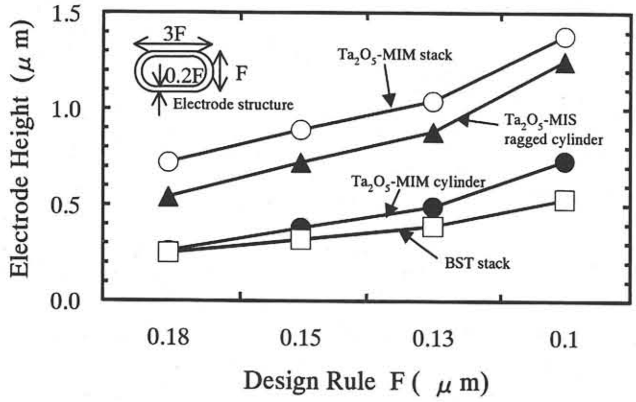

Fig.1 Electrode height as a function of the minimum design rule (F). T_{eq} is assumed to be 3.0 nm (Ta_2O_5-MIS), 1.0 nm(Ta_2O_5-MIM) and 0.4 nm(BST) .

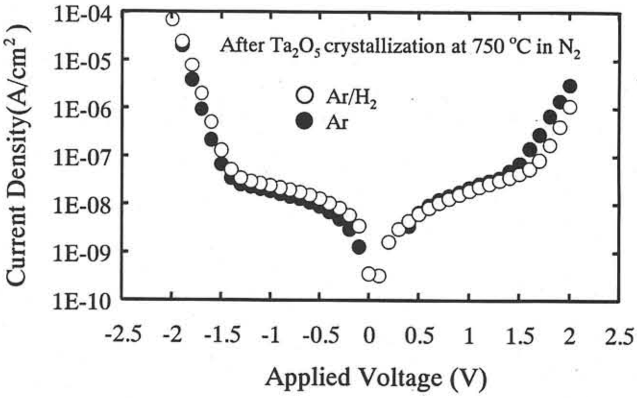

Fig.2 I-V characteristics of crystallized $Ru/Ta_2O_5/Ru$ capacitor with T_{eq} of 0.9 nm.

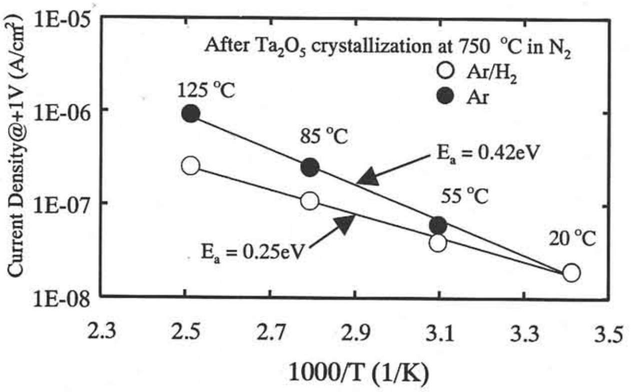

Fig.3 Arrenius plot of the leakage current at +1V top electrode bias.

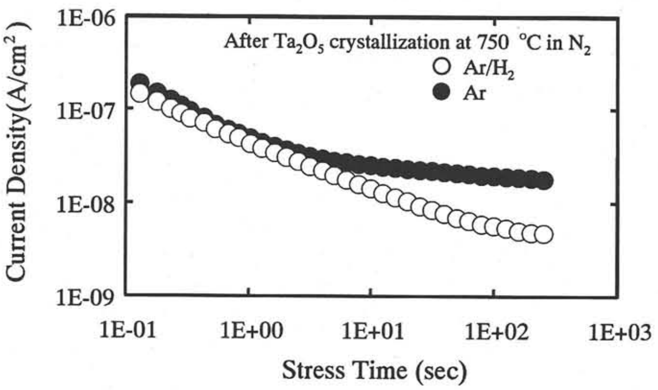

Fig. 4 Time dependence of current density characteristics at room temperature under a bias of +1V on the top electrode.

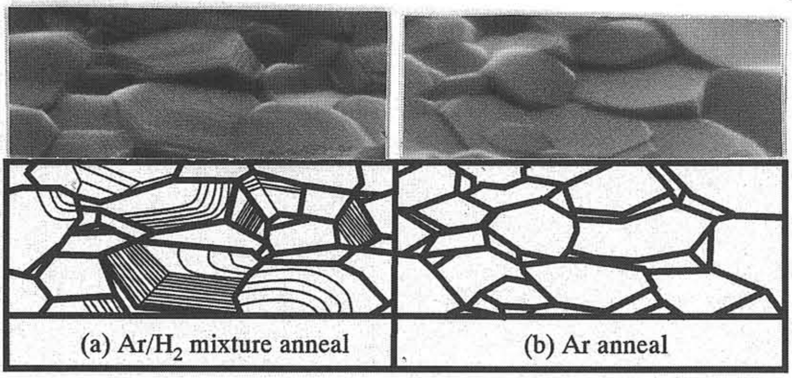

Fig.5 Perspective SEM views and traces of Ru surface.

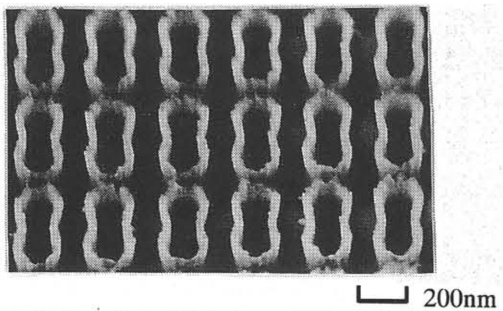

Fig.6 Perspective SEM view of Ru cylindrical electrode array.

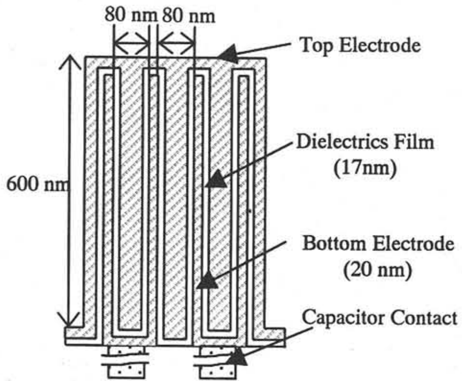

Fig.7 Schematic cross section of 0.1 μ m DRAM cell structure.