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Fabrication of the $Si/Al_2O_3/SiO_2/Si$ Structure by Using the O_2 Annealed Al_2O_3/Si Structure

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1. Introduction

SOI wafers were used not only for the ULSI applications, but also for the other one such as sensors. Multi-stacked SOI structure have potential for these sensors and MEMS (Micro Electro Mechanical system) applications. However, it is difficult to obtain multi-stacked SOI structures using these fabrication methods such as SDB and SIMOX. SOI structures of double-heteroepitaxial Si/γ-Al_2O_3/Si grown by LP-CVD,[1] UHV-CVD[2] and Si_2H_6 gas-source MBE[3] were reported. The SOI structure with Al_2O_3 was applied to a high-temperature-operated pressure sensor[4].

There is the remained problem that Si top layer morphology of SOI structure fabricated by the UHV-CVD system depends on the Al_2O_3 layer thickness.[5] As Al_2O_3 thickness is more than 30 nm, the endurance voltage property is excellent, while Si top layer is rough. As Al_2O_3 thickness is less than 10 nm, Si top layer is smooth surface, while the endurance voltage property is not good.

In this work, the formation of the SiO_2 layer such as $Al_2O_3/SiO_2/Si$ structure in the interface between Al_2O_3 and Si was investigated to improve the problem of the insulation. Moreover, Si growth was carried out on the $Al_2O_3/SiO_2/Si$ structure. Then the high crystalline quality of SOI wafer was fabricated.

2. $Si/Al_2O_3/SiO_2/Si$ Formation

Al_2O_3 and Si growth were carried out using the UHV-CVD system as reported previously.[5-7] $Si/Al_2O_3/SiO_2/Si$ structure was prepared by the following fabricating sequence. (1) Al_2O_3 growth at a lower temperature of 900℃ was performed on a 2 inches p-type Si(100)to get good surface morphology. (2) The wafer was annealed in O_2 atmosphere to fabricate the SiO_2 layer at the interface between Al_2O_3 and Si. Annealing was performed at 1000℃ for 120 min. (3) To improve crystallinity of Al_2O_3 films, Al_2O_3 growth at a high temperature of 1000℃ was performed on the $Al_2O_3/SiO_2/Si$ structure. (4) Single-crystal Si(100) films were epitaxially grown on the $Al_2O_3/SiO_2/Si$ structure by Si_2H_6 at 1000℃.

3. Results and Discussion

Figure 1 shows the AES depth profile of the sample with O_2 anneal using a 15 nm thick Al_2O_3 films. In case of the O_2 annealed one, SiO_2 was observed at the interface between the Al_2O_3 layer and the Si substrate. Figure 2 shows the characteristics of leakage current. The 11 nm thick Al_2O_3 film had poor electric resistance (the endurance voltage was 10V), whereas the 11 nm thick Al_2O_3 films with 63 nm thick SiO_2 layer in the interface between Al_2O_3 and Si had good electric resistance (the endurance voltage was 50V). RHEED pattern of the Si layer on $Al_2O_3/SiO_2/Si$ shows the streaky patterns shown in Fig3 (a), which indicates that the crystalline is good. Figure 3(b) shows the surface morphology of Si top layers with $Al_2O_3/SiO_2/Si$. The thermal expansion coefficient of Si, Al_2O_3 and SiO_2 has the relation such as $SiO_2<Si<Al_2O_3$. The relaxation of the distortion by the SiO_2 layer in the interface between Al_2O_3 and Si was examined. The relaxation of the distortion may be improved by control of SiO_2 layer and Al_2O_3 film thickness. The defect density of Si top layer of $Si/Al_2O_3/SiO_2/Si$ structure decreased to a half compared with Si top layer of $Si/Al_2O_3/Si$ structure. It is considered that this decrease may be caused by the effect of the relaxation of the distortion by the SiO_2 layer in the interface between Al_2O_3 and Si, but requires further study for clarification. Figure 4 shows characteristics of nMOS FET, and indicates electrical properties of the MOS FET as the same as that on Si substrate.

The high quality SOI wafers by this epitaxial growth enable to use for sensors and display devices with CMOS IC on the same chips. The CMOS fabrication process using this SOI structure as well as the SOI wafer fabrication process was studied, and the operation of the CMOS integrated circuits on it was demonstrated.

4. Conclusions

The formation of the SiO_2 layer in the interface between Al_2O_3 and Si to improve the insulation was carried out using O_2 anneal at 1000℃. As the result, Al_2O_3/Si structure was changed to

$Al_2O_3/SiO_2/Si$ structure in case of thin Al_2O_3 films. By the fabricating the $Al_2O_3/SiO_2/Si$ structure, the endurance voltage property was more excellent than Al_2O_3/Si structure from 10 V to 50 V. Moreover, Si growth was carried out on the $Al_2O_3/SiO_2/Si$ structure. The Si top layer morphology was very smooth. Then, the high crystalline quality of SOI wafer was fabricated, and good properties of MOS devices were obtained.

References

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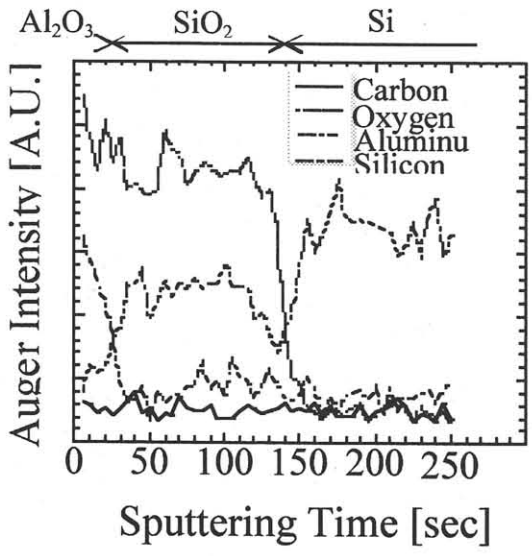

Fig.1 AES depth profile of Al2O3/Si with O2 anneal.

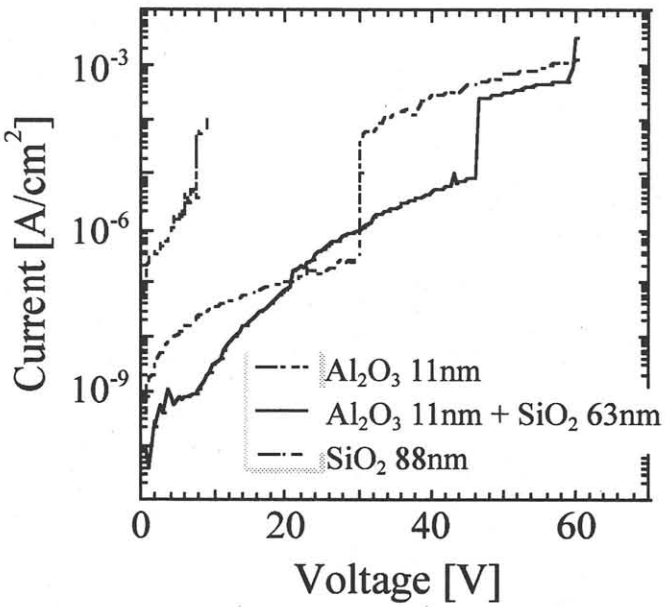

Fig.2. Properties of brake-down voltages of various insulator/Si samples.

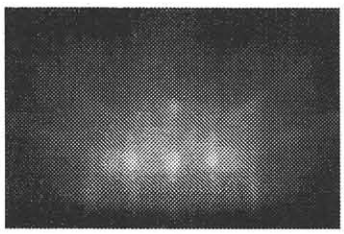

Fig.3 (a) RHEED of Si/Al2O3/SiO2/Si.

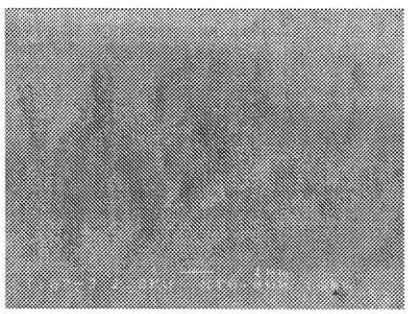

Fig. 3(b) SEM of Si/Al2O3/SiO2/Si.

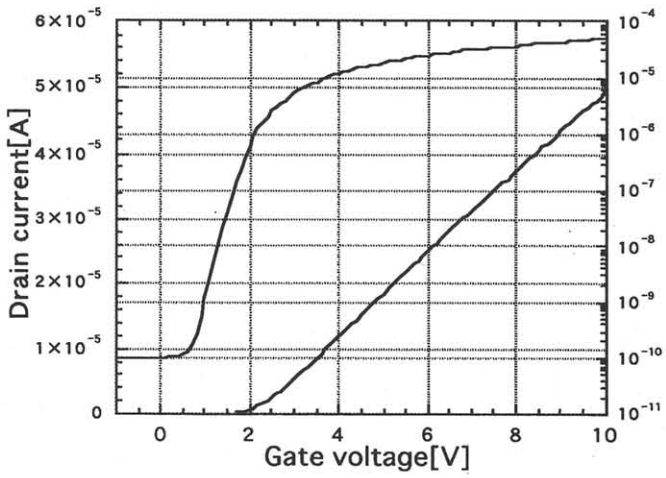

Fig.4. I_D-V_G of nMOS FET on SOI.