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Invited

Transport Properties in Sub-10-nm-gate EJ-MOSFETs

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1. Introduction

For more than 20 years the miniaturization of MOSFETs has been the driving force behind their improved performance and the higher integration. In the future, we will maintain this progress rate to ensure the semiconductor market grows. In the research level sub-50-nm-gate devices have already been reported [1]. However, when the gate length approaches the 10-nm level or less, what will happen in the transistor operation. Since this gate length is close to the wavelength of conducting carriers, quantum effects such as tunneling or interference may appear in MOSFET characteristics. It is our aim to experimentally study the transport properties in this regime.

To do this, we have proposed a test structure, an electrically variable shallow junction MOSFET (EJ-MOSFET) [2], which emulates conventional MOSFET operations. Since the EJ-MOSFET has electrically induced ultrashallow source/drain junctions, its structure has an excellent tolerance for short-channel effects. By using a 10-nm-level lithography technique with an ultrahigh resolution resist (calixarene), we achieved a minimal gate length of 8 nm. In this paper, we report the experimental results of transport properties in ultrasmall EJ-MOSFETs.

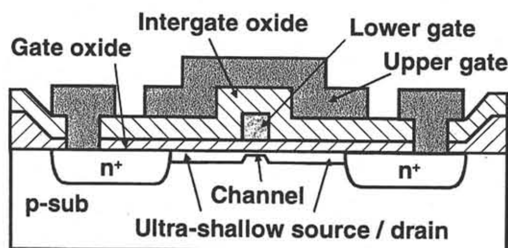

Figure 1: Schematic cross-section of an EJ-MOSFET.

2. EJ-MOSFET Structure

Figure 1 shows a schematic cross-section of an EJ-MOSFET. This structure has two gates: an Au/Al upper gate and a phosphorus-doped poly-silicon lower gate. These gates were insulated by a 25-nm-thick intergate oxide film grown by low-pressure chemical vapor deposition. The (100)-oriented silicon substrate was doped with the boron-concentration of $2 \times 10^{18}\text{cm}^{-3}$. The gate oxide thickness was 5 nm.

A positive upper-gate bias induced inversion layers at the silicon surface. These inversion layers worked as

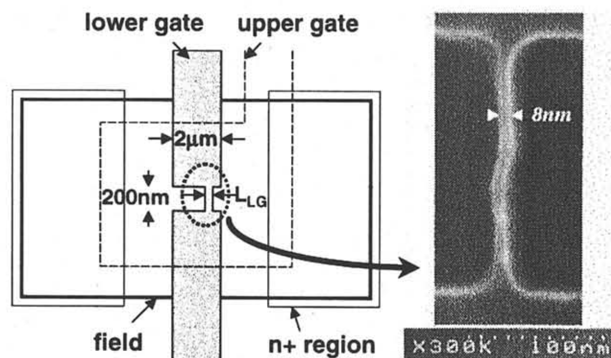

Figure 2: Schematic top view of an EJ-MOSFET and SEM top view of the poly-silicon lower gate

source/drain regions like an ILD-MOSFET [3]. The lower gate, which corresponds to the "gate" in conventional MOSFETs, controlled the current between the source and the drain. Since the source/drain junction depth was extremely shallow (typically 5 nm in depth), this structure had an excellent tolerance for short-channel effects. Figure 2 shows a schematic top view of an EJ-MOSFET and an SEM top view of the poly-silicon lower gate. We can see uniform poly-silicon pattern with the lower-gate length (L_{LG}) of 8 nm. The lower gate was patterned by using electron-beam direct writing on the calixarene resist followed by reactive-ion etching with CF_4 gas.

3. Transport Properties

Figure 3(a) shows the current-voltage characteristics at $L_{LG} = 8$ nm. Although the saturation currents had a slight drain bias dependence, the ultrasmall transistor operated at 300 K. Figure 3(b) shows the subthreshold characteristics for various L_{LG}s at 300 K. Although the threshold voltage roll-off and the increase in subthreshold swing (S-factor) were observed with decreasing L_{LG}, the device kept a sufficiently large ON/OFF current ratio even at $L_{LG} = 8$ nm.

To study the transport properties, we measured the temperature dependence of subthreshold currents for 5 K $\leq T \leq$ 300 K and 8 nm $\leq L_{LG} \leq$ 100 nm. Figure 4(a) shows the measured temperature dependence of subthreshold currents at $L_{LG} = 8$ nm. At $T > 100$ K the S-factor decreased against a decreasing T with the relationship $S \propto T$. At $T < 100$ K, on the other hand, the S-factor almost stayed constant against T. For

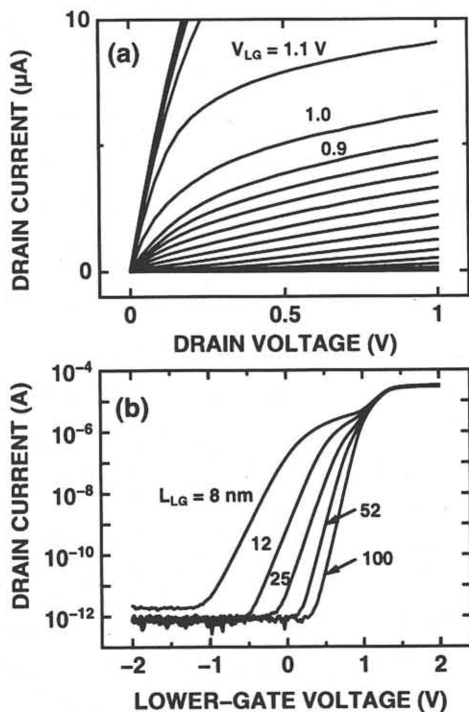

Figure 3: Current-voltage characteristics at $L_{LG} = 8$ nm (a) and subthreshold characteristics (b) at 300 K. The upper gate voltage of 13 V and the drain voltage of 0.5 V were applied. At $V_{LG} \geq 1$ V the channel beneath the longer portion in the lower gate turned on, and the drain currents showed stepwise increase

$L_{LG} \geq 50$ nm, we did not observe such T-independent behavior of the S-factor at $T > 10$ K. If we define T_c as the temperature below which the S-factor stayed constant, T_c showed a significant increase for $L_{LG} < 25$ nm with decreasing T and reached 77 K at $L_{LG} = 8$ nm. In addition T_c approached the relation $T_c \propto 1/L_{LG}^2$ [4]. Extrapolation of the relation gave a $T_c = 300$ K for $L_{LG} = 4$ nm.

Figure 4(b) shows the calculated results for Fig. 4(a). The one-dimensional calculation including tunneling effects was performed with the surface potential distribution obtained by the two-dimensional device simulation. The calculation reproduced the experimental results in Fig. 4(a) except for the discrepancy of 0.5 V in the threshold voltage. Figure 4(c) separately plots the thermal and tunnel components in the calculated currents shown in Fig. 4(b). For $T > 100$ K, the thermal process was dominant and the resulting total currents had strong temperature dependence. For $T < 100$ K, on the other hand, the tunneling process became dominant and caused the T-independent nature of the S-factor. In the case of a rectangular barrier, the tunneling probability is proportional to $exp(-\alpha w\sqrt{h})$, where α, w, and h are a constant, a barrier width, and a barrier height, respectively. When w decreases, the tunneling probability increases, leading to an increase in T_c. For $w = 6$ nm, T_c reaches 300 K. Taking into account that the tunneling process has a weaker h-dependence than the thermal process, the process degrades the S-factor and prevents low-voltage operations. The direct tunneling phenomena will be one of the physical limitations in room-temperature MOSFET operations in this regime.

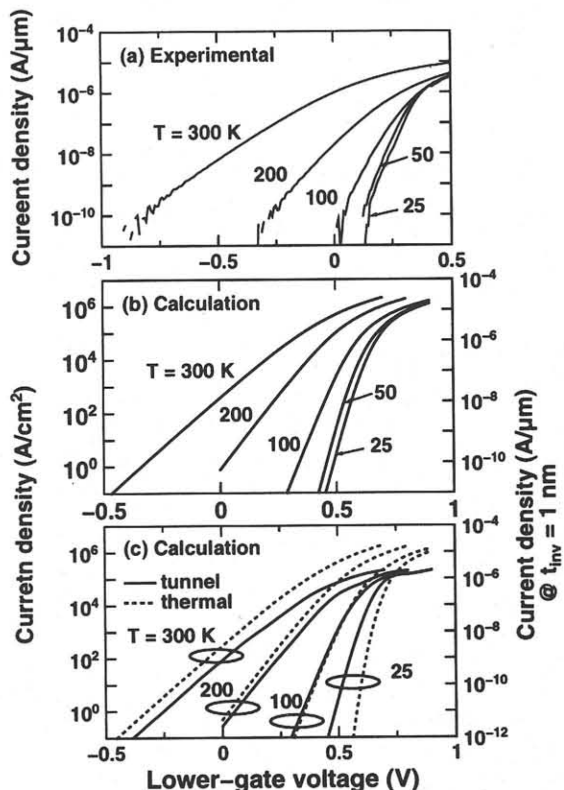

Figure 4: (a): Temperature dependence of subthreshold currents for $L_{LG} = 8$ nm . (b): Calculated results for (a). (c): Plots of thermal and tunneling components in (b).

5. Conclusion

We confirmed the transistor operation of EJ-MOSFETs with the gate length of 8 nm at 300 K. In this device we firstly found direct tunneling phenomena from the source to the drain at $T \leq 77$ K. In addition we showed that such a tunneling process is dominant in the subthreshold region and degrades the S-factor in the 5-nm regime even at 300 K.

Acknowledgments

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References

[1] M. Ono et al., IEDM Tech. Dig., p. 119 (1993).

[2] H. Kawaura et al., Ext. Abs. of SSDM, p. 22 (1996).

[3] H. Noda et al., IEDM Tech. Dig., p. 123 (1993)

[4] If T-independent nature is caused by tunneling process through a rectangular barrier, T_c is expressed in this formula at large T_c.