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# Influence of Intrinsic Current Fluctuation in Very Small Si-MOSFETs

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## 1. Introduction

The unlimited miniaturization of Si-MOSFETs is being pursued at various leading research laboratories. As a result, fluctuations of various device characteristics could be of critical importance for future large-scale integration. The threshold voltage fluctuation, among others, is a typical issue [1-2]. Nevertheless, almost no attention has been paid on the current for such very small devices. The reduction of the device width, however, may also introduce the current fluctuation because of the drastic decrease of the channel electrons.

In the present paper, we investigate the current fluctuation in Si-MOSFETs via Monte Carlo (MC) simulations as a function of the device width $W$. We demonstrate that the current fluctuation indeed becomes significant as the device width shrinks into deep sub-$\mu$m regimes. This fluctuation results from the graininess of electrons in the channel and is closely related to the thermal noise in high-doped regions beside the channel. More importantly, this fluctuation is intrinsic in the sense that it cannot be removed in principle.

## 2. Simulation Method

The present analyses are carried out under typical Si-MOSFET structures with the effective channel lengths of $L_{\rm eff}$ = 300 and 40 nm. Notice that, depending on the channel length, the electrons do transport diffusively or quasi-ballistically. The device parameters employed for the Monte Carlo simulations are summarized in Table 1.

Simulations are performed by using the ensemble Monte Carlo method under the fixed potential profile obtained from the conventional Drift-Diffusion simulation [3]. The Monte Carlo method employed here is a simple and conventional one; the analytical (nonparabolic) electronic band structure and the material parameters for Si known in the literature are used [4]. The periodic boundary condition is assumed at the source and drain contacts so that the number of all simulating electrons inside the device does not change. The number of simulating electrons is determined by the device width $W$ provided that each simulating electron corresponds to a *real* electron. Electron kinetics is simulated for several ten ps and the device characteristics, such as the drain current and the current variance, are sampled after a transient of about 5 ps. The channel current $I(t)$ at time $t$ is evaluated using the Ramo-Shockley formula [5] and recorded at every 1 fs.

| | | |
|---|---|---|
| channel length (nm) | 300 | 40 |
| oxide thickness (nm) | 10 | 3.5 |
| substrate impurity ($cm^{-3}$) | $7 \times 10^{17}$ | $2 \times 10^{18}$ |
| junction depth (nm) | 80 | 10 |

Table 1: Device parameters employed for the present Monte Carlo simulations.

## 3. Results and Discussion

A typical drain voltage dependence of the drain current $I_{\rm ave}$ and the variance (fluctuation) of the drain current $\langle \delta I^2 \rangle$ is shown in Fig 1. Notice that the current variance is almost independent of the drain voltage. This implies that the current fluctuation is dominated by the (quasi-equilibrium) thermal noise, which is independent of the voltage, in high-doped regions beside the channel. The details of our study on the spatial origin of this current noise under MOSFET structures will be reported elsewhere. One could easily conjecture from Fig. 2 how significant the current fluctuation could be. Figure 2 shows the statistics of the drain current fluctuation in Si-MOSFET with $L_{\rm eff}$ =40 nm. The statistics is taken by accumulating the drain current at many (typically, thousands) instant times.

Under the quasi-equilibrium situations, the thermal noise is essentially equivalent to the shot noise [6]. Thus, the current variance $\langle \delta I^2 \rangle$ may be approximated by using the well-known formula of the shot noise: $\langle \delta I^2 \rangle = 2\,q\,I_{\rm ave}\,\Delta f$, where $q$ is the magnitude of the electronic charge and $\Delta f$ the frequency band width. Since the averaged drain current is proportional to the device width $W$, the normalized standard deviation of the drain cur-

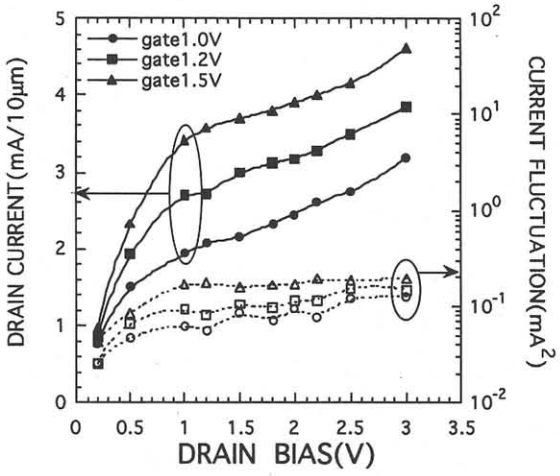


Figure 1: Typical drain voltage dependence of the drain current (left scale) and the variance of the drain current (right scale) $\langle \delta I^2 \rangle$ in the n-channel Si-MOSFET with $L_{\rm eff}$ =40 nm.

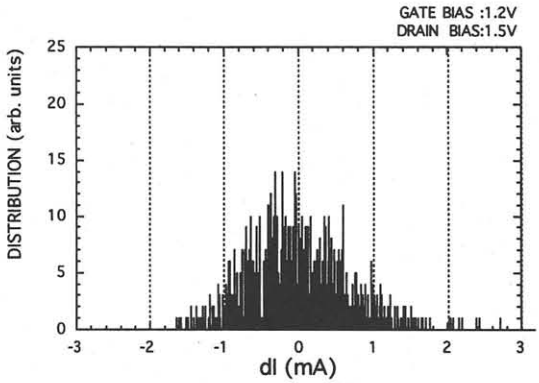


Figure 2: Statistics of the drain current fluctuation in Si-MOSFET with $L_{\rm eff}$ =40 nm under $V_{\rm g} = 1.2$ V、 $V_{\rm d} = 1.5$ V. The averaged current $I_{\rm ave}$ is 3 mA/10 $\mu$m.

rent is given by

$$\frac{\sqrt{\langle \delta I^2 \rangle}}{I_{\rm ave}} = \sqrt{\frac{2\,q\,\Delta f}{I_{ave}}} \propto \frac{1}{\sqrt{W}} \,. \qquad (1)$$

Therefore, the normalized standard deviation of the drain current is inversely proportional to $\sqrt{W}$. The normalized standard deviation obtained from MC simulations is plotted as a function of the width $W$ in Fig. 3. The normalized standard deviation indeed increases as the device width shrinks and well approximated by Eq. (1). Notice that deviation attains even several ten percent when the device width is reduced into deep sub-$\mu$m.

## 4. Conclusions

The current fluctuation under Si-MOSFET structures has been studied with the Mónte Carlo simulations. It

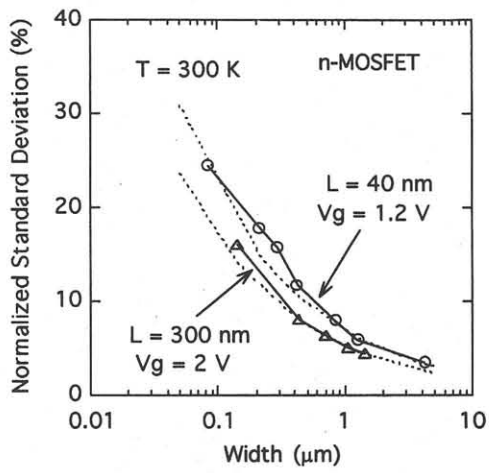


Figure 3: Normalized standard deviation of the drain current as a function of the width $W$ of Si-MOSFETs for the channel length of $L_{\rm eff}$ =40 and 300 nm. The dotted line is the theoretical prediction described in the text.

has been demonstrated that, as the absolute number of the channel electrons decreases, the relative magnitude of the current fluctuation (variance) increases with respect to the averaged current. As a result, the normalized standard deviation of the current variance attain several ten percent when the device width is reduced into deep sub-$\mu$m.


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