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Improvement in Low Temperature CMOS Performance Using Retrograded Channel Profiling

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Introduction: Low temperature CMOS has been examined by various groups as a means of improving device and circuit performance [1-2]. When the operating temperature is lowered, subthreshold slope decreases and current drive increases. In order to fully optimize CMOS for low temperature operation, changes from a conventional room temperature process flow are necessary [3]. In this paper it will be shown that retrograding the doping profile in the channel region leads to an 80% improvement in saturation current and a 55% reduction in propagation delay at 78 K.

Process Details: A series of NMOS and PMOS devices with CMOS ring oscillators were fabricated. Gate oxide thicknesses of 7 and 5 nm were used. E-beam lithography was employed to define gate lengths down to 0.2 μm. Dual polarity polysilicon and high dose source/drain extension implants were used to minimize freezeout effects. Table 1 summarizes the different threshold implants of the NMOS devices. Since the mobility at low temperature is limited by charge impurity scattering [4], a low surface doping concentration is desired. But to maintain good short channel behavior, the doping level must be high within the depletion region. Hence a retrograded doping profile is ideal for low temperature operation. By using indium implantation and rapid thermal annealing (instead of boron implantation and furnace annealing), redistribution of the threshold implant profile can be minimized.

Device Results: Testing was performed on a Lakeshore Cryostat dewar at temperatures of 78 K, 150 K, 218 K, 300 K, and 343 K. Good I-V characteristics were obtained down to effective channel lengths of 0.15 μm. Figures 1 and 2 show the I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics of a 0.15 μm NMOS device at different temperatures. The saturation current improves linearly as the temperature is lowered (Figure 3) and shows no freezeout. The effect of the NMOS V_{th} implant on the saturation current is indicated in Figure 4. By using indium implantation and RTA annealing to retrograde the doping profile in the channel region, the saturation current at 78 K improves by an additional 10-30%, depending on the energy and dose of the implant. At lower power supply voltages (Figure 5), further improvement is achieved due to reduced scattering effects. The short channel effects of the indium implanted wafers are similar to the boron implanted wafers (Figure 6).

Circuit Results: Figure 7 shows the propagation delay of an 83 stage, 2-input NOR ring oscillator at different temperatures. Again, the indium retrograded profile shows better improvement than the boron profile at 78 K (Figure 8). The amount of improvement here is less than the I_{dsat} improvement because the threshold voltage shift from room to low temperature cannot be taken into account. However, the indium ring oscillator at low temperature can be normalized to the boron ring oscillator at room temperature because the threshold voltages for each circuit are similar (Figure 9). This results in a 2x improvement in delay. Additional optimization of the PMOS devices should lead to an even greater performance at low temperature.

Conclusion: Although retrograded profiling has received mixed reviews at room temperature [5-6], significant improvement is expected at low temperature due to improved mobility. Since the channel doping concentration must be reduced to counteract the increase in threshold voltage at low temperature, retrograding the channel doping profile should be done to maintain good short channel behavior. By correctly adjusting the threshold voltage and lowering the doping concentration near the surface, a 2x improvement in circuit performance can be easily achieved. This still makes temperature an attractive scaling parameter for improving the performance of CMOS circuitry, especially as fundamental limits are being approached in both linewidth resolution and oxide thickness.

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3. C. Hwang, C. Jenq, B. Hammond, J. Gillick, and J. Woo, *Second European Workshop on Low Temperature Electronics*, pg. 193-197, 1996.
4. J. Watt and J. Plummer, *Symposium on VLSI Technology*, pg. 81-82, 1987.
5. G. Shahidi, et. al., *IEEE Electron Device Letters*, pg. 466-468, 1993.
6. S. Venkatesan, J. Lutze, C. Lage, and W. Taylor, *IEDM Technical Digest*, pg. 419-422, 1995.

Wafer	t_{ox} (nm)	NMOS V_{th} Implant	Anneal
B1	7	Boron: 4 x 10^{12} cm^{-2} @ 40 keV	Furnace (950°C, 30 min)
IN1	7	Indium: 4 x 10^{12} cm^{-2} @ 300 keV	RTA (950°C, 2 min)
IN2	7	Indium: 8 x 10^{12} cm^{-2} @ 300 keV	RTA (950°C, 2 min)
IN3	7	Indium: 1 x 10^{12} cm^{-2} @ 150 keV	RTA (950°C, 2 min)
B2	5	Boron: 8 x 10^{12} cm^{-2} @ 40 keV	RTA (950°C, 30 sec)
IN4	5	Indium: 6 x 10^{12} cm^{-2} @ 300 keV	RTA (950°C, 30 sec)

Table 1: Oxide thickness, NMOS V_{th} implant dose, and annealing conditions for the fabricated devices.

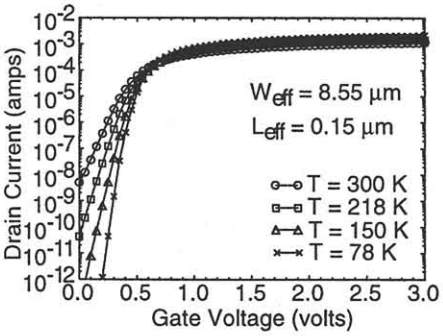

Figure 1: I_{ds}-V_{gs} characteristics of an 8.55 x 0.15 µm NMOS transistor (Wafer B1) at 300 K, 218 K, 150 K, and 78 K.

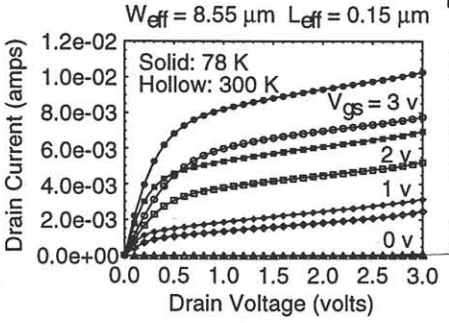

Figure 2: I_{ds}-V_{ds} characteristics of an 8.55 x 0.15 µm NMOS transistor (Wafer B1) at 300 K and 78 K.

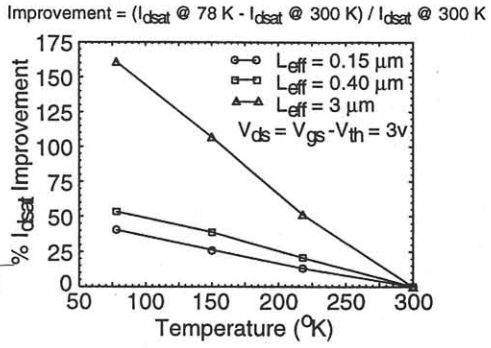

Figure 3: Improvement in saturation current versus temperature (Wafer B1) for long and short channel NMOS devices.

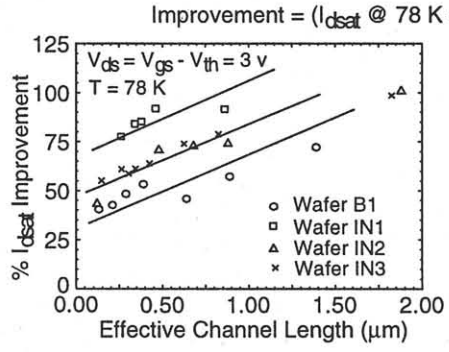

Figure 4: Improvement in saturation current for standard (Wafer B1) and retrograded (Wafers IN1-IN3) profiles.

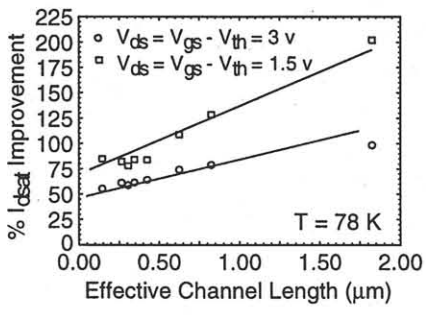

Figure 5: Improvement in saturation current versus power supply voltage for a retrograded profile. (Wafer IN3).

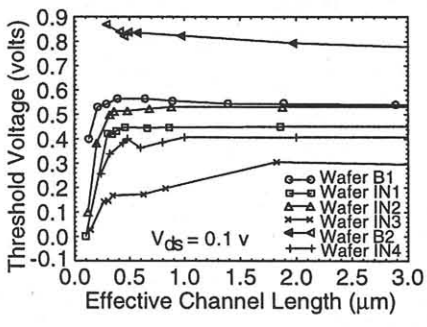

Figure 6: Threshold voltage versus channel length for the NMOS devices at 78 K. Vth is defined here as the gate voltage corresponding to (10 nA x W/L) drain current.

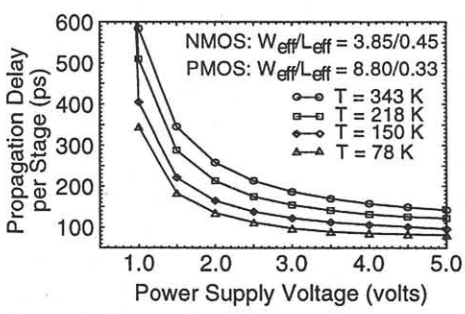

Figure 7: Propagation delay versus power supply voltage of an 83 stage 2-input NOR ring oscillator (Wafer IN4). The two inputs are tied together at each stage. The output is driven through a buffer into the 50 Ω input of an oscilloscope.

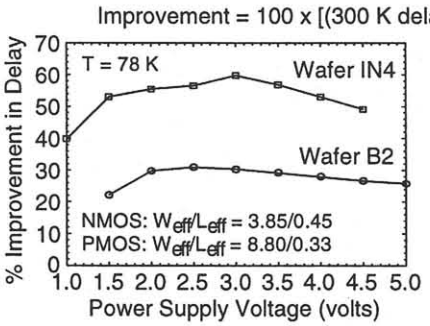

Figure 8: Improvement in propagation delay versus power supply voltage of an 83 stage 2-input NOR ring oscillator at 78 K

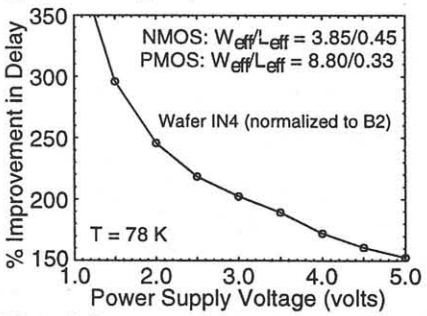

Figure 9: Improvement in propagation delay of an 83 stage 2-input NOR ring oscillator. The low temperature indium data (NMOS Vth = 0.40v) has been normalized to the room temperature boron data (NMOS Vth = 0.44v)