Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 124-125

Uni-Directional HV MOS Device Modeling for Circuit Simulation

T. Myono, E. Nishibe, S. Kikuchi, K. Iwatsu

MOS-LSI Division, SANYO Electric Co. Ltd.,
1-1-1 Sakata, Oizumi-machi, Oragun, Gunma 370-0596, Japan
Phone: +81-276-61-8562 **Fax:**+81-276-61-8836 **E-mail:**myon003877@swan.sanyo.c

1. Introduction

We have developed several kinds of HV MOS devices whose device structures and doping levels in the offset region are different. Representative of these are 80V and 45V HV MOS devices. The 80V HV MOS device is bi-directional with offset regions in both drain and source, and we have already described its SPICE model [1, 2] based on BSIM3v3 [3]. The n-channel 45V HV MOS device, on the other hand, is uni-directional, and has an offset region only in the drain. Fig.1 shows its structure. The bi-directional HV MOS model we proposed necessarily includes the source resistance which the uni-directional HV MOS does not have, and hence if we apply the bi-directional HV MOS model and its parameter extraction technique directly to the uni-directional HV MOS model, we have to compensate for the part of the drain current caused by the source resistor model. However this compensation makes it difficult to express the Gm-reduction as the gate-source voltage (V_{gs}) increases, which is the inherent phenomenon of the HV MOS device, and this causes large discrepancies between the measured and simulated I-V characteristics of the uni-directional device. We propose a modeling technique for the uni-directional device. We use the same model for the uni-directional HV MOS device as for the previously reported bi-directional HV MOS model [1, 2], but we adopt a new parameter extraction technique. Agreement of the simulated and measured results shows that our proposed method can model the uni-directional HV MOS device accurately.

2. Uni-directional HV MOS device technology

Fig.1 shows the structure of the 45V n-channel HV MOS device we have developed, and it has n^- offset region of low doping concentration only in drain to realize large breakdown voltage only in drain-source direction. When the drain-source voltage (V_{ds}) is applied to the HV MOS device, the depletion region grows in the n^- offset region, and due to this depletion region growth the channel and n^- offset region are separated. Then the channel voltage at the drain terminal saturates with a small voltage which reduces the effective voltage across the HV MOS channel and hence improves the breakdown voltage between drain and source. Note that since the channel voltage at the drain terminal saturates in the triode region, the Gm is reduced as the V_{gs} increases.

3. Application of bi-directional HV MOS modeling

Step II in Table 1 shows the parameters obtained by applying the bi-directional HV MOS model and parameter extraction technique to the uni-directional HV MOS device, and Fig.2 shows a comparison between simulated and measured I-V characteristics. We see that the Gm-reduction of the uni-directional HV MOS device is not expressed correctly. In [1] we express correct Gm-reduction for the bi-drectional HV MOS by making *AGS* be a large negative value. However, for the uni-directional HV MOS modeling, we have to take care of both Gm-reduction and compensation of the part of the drain current due to the source resistor model, and we have found that just adjusting the value of *AGS* can not take care of both simultaneously because making *AGS* be a large negative value may lead to correct Gm-reduction but it also causes a larger current due to the source resistor model.

4. uni-directional HV MOS modeling technique

Let us consider to use equations (9)-(15) of the bi-directional HV MOS model shown in our previous paper [1] as the base for uni-directional HV MOS model. V_{ds}' of equation (13) in [1] stands for a channel voltage at the drain terminal, and V_{dsat} in equation (9) in [1] has to be optimized to the channel-saturation voltage at the drain terminal with *AGS*. V_{rs} in equation (14) in [1] represents a voltage drop across the source resistance, and since V_{rs} is necessarily included in the bi-directional HV MOS model, it can not be eliminated from the model equations and we have to compensate for it. Now let us define the drain current I_{dsr0} where the part of the drain current caused by V_{rs} is compensated:

$$G_{dsr0} = \mu_{eff} C_{ox} \frac{W}{L}\left(V_{gs} - V_{th} - \frac{V_{ds}'}{2}\right) \quad (1)$$

$$I_{dsr0} = \frac{G_{dsr0} V_{ds}'}{1 + G_{dsr0} R_{ds}} \quad (2)$$

Let us define I_{vrs} as the part of the drain current due to V_{rs}, and we obtain the following:

$$I_{ds} = I_{dsr0} - I_{vrs} \quad (3)$$

5. parameter extraction technique

We propose a parameter extraction technique for the uni-directional HV MOS model to express its Gm-reduction by R_{ds} and its I_{vrs}-compensation by *AGS*. BSIM3v3 SPICE model combines source and drain resistances as R_{ds} as a function of V_{gs} as follows:

$$R_{ds} = \frac{RDSW\left(1 + PRWG \cdot V_{gs}\right)}{W} \quad (4)$$

R_{ds} is used explicitly to express G_{dsr0} in eq. (2), and it hardly affects the V_{dsat}. Note that G_{dsr0} has R_{ds} in its denominator,

and hence the accurate Gm-reduction can be expressed for I_{dsr0}, I_{ds} and I_{vrs} mathematically by making R_{ds} be a function of V_{gs}. Also note that *AGS* is just used for I_{vrs}-compensation this time, and the proposed parameter extraction procedure is as follows:

1) First, extract all BSIM3v3 parameters by the standard method (step I in Table 1).
2) Then set the value of *VSAT* to a large value (e.g., 1E9) to assume the long channel device.
3) Also set the value of *PCLM* to 0 to make the Gm-reduction in the saturated region larger than that in the triode region because in our model R_{ds} provides the Gm-reduction both in the triode and saturation regions, but we need it only in the saturation region.
4) Optimize *U0*, *RDSW*, *PRWG*, *AGS*, and *DELTA* together in all the triode region (up to close to the saturation region) i.e., from (V_{ds}=0V, V_{gs}=1.93V) to (V_{ds}=20V, V_{gs}=45V). *RDSW* and *PRWG* have to be optimized such that R_{ds} express Gm-reduction of I_{dsr0} while *AGS* has to be optimized such that A_{bulk} and V_{dsat} compensate for I_{vrs}.

Step III in Table 1 shows the extracted parameter values according to the above procedure, and Fig.3 shows the comparison between the measured and simulated I-V characteristics of the uni-directional HV MOS. We see that a good agreement is obtained between the measured and simulated results. Fig.4 shows the calculated R_{ds} as a function of V_{gs}. R_{ds} of ordinary devices does not depend on the value of V_{gs}. Note that there are some discrepancies in the operating region where the measured drain conductance (Gds) is negative, but we will not use this region for our circuit design.

References

[1] T. Myono, S. Kikuchi, K. Iwatsu, E. Nishibe, T. Suzuki, Y. Sasaki, K. Itoh and H. Kobayashi, "High-Voltage MOS Device Modeling with BSIM3v3 SPICE Model, "IEICE TRANS. ELECTRON, vol.E82-C, No.4, April 1999, pp630-637.

[2] T. Myono, E. Nishibe, S. Kikuchi, K. Iwatsu, T. Suzuki, Y. Sasaki, K. Itoh and H. Kobayashi: 'Modeling and parameter extraction technique for high-voltage MOS device', ISCAS99, (accepted).

[3] Y. Cheng, M.-C. Jeng, Z. Liu, J. Hubg, M. Chen, P. K. Ko and C. Hu: 'A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation', IEEE Electron Devices, vol.44, no.2, Feb. 1997, pp.277-287

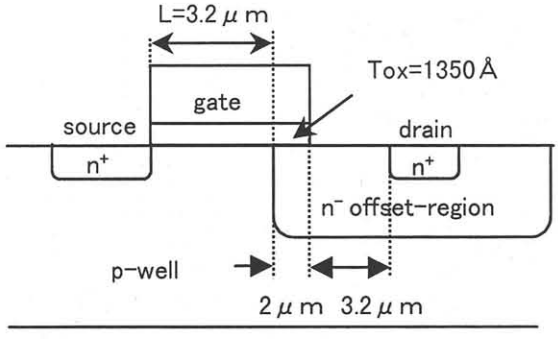

Fig. 1 Schematic structure of the uni-directional N-channel HV MOS device.

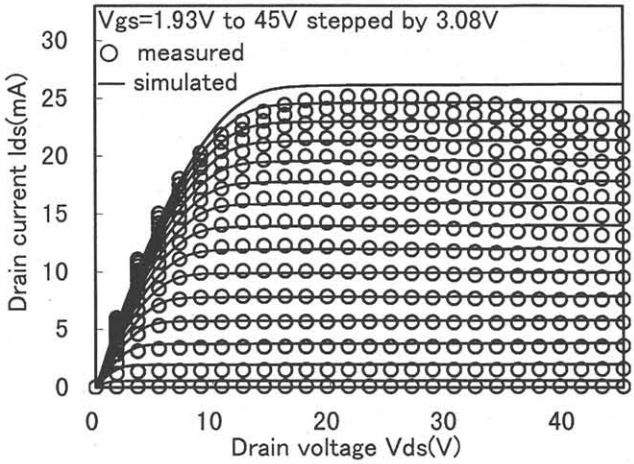

Fig. 2 Comparison between measured and simulated (with the bi-directional HV MOS model) I-V characteristics.

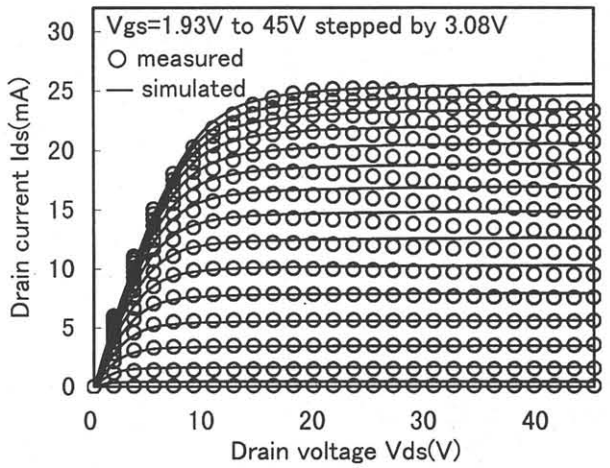

Fig. 3 Comparison between measured and simulated (with the uni-directional HV MOS model) I-V characteristics.

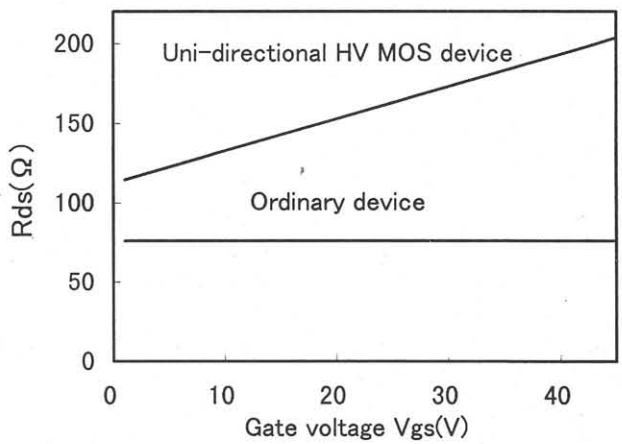

Fig. 4 Calculated R_{ds} as a function of V_{gs}.

Table 1 Extracted BSIM3v3 parameter values for each step.

	AGS	U0	PCLM	RDSW	PRWG
Step I	0.084	616	11.7	3.8E3	0.0
Step II	-0.036	616	11.7	3.8E3	0.0
Step III	-0.077	588	0.0	5.5E3	0.018