Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 134-135

New Guidelines of Optimizing SALICIDE Structure for High Speed CMOS LSI

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1. Introduction

SALICIDE technology has been widely used for CMOS logic LSI since low sheet resistivity of gate electrodes and reduced parasitic source/drain resistance can be realized. While the sheet resistivity of gate and source/drain electrodes is lowered with increasing silicide layer thickness, the contact resistivity of silicide/silicon interface shows reversed behavior since excess silicidation consumes highly doped region of diffusions. Thus, it is significant to optimize the silicide layer thickness for the performance of CMOS, while taking into account its impact on gate RC delay and parasitic source/drain resistance.

In this paper, a simple optimizing procedure based on an analytical model is presented.

2. Electrical Parameters of Salicided MOSFET

Each resistive component of Salicided MOSFET shown in Fig. 1 as function of t_{CoSi2}, the silicided layer thickness, is presented as follows. The measured MOSFET is fabricated with 0.15 μm Co SALICIDE technology.

Both ρ_{sG} and ρ_{sS}, the sheet resistivity of gate electrodes and source/drain electrodes, are inversely proportional to t_{CoSi2} as shown in Fig. 2(a) and (b). Thus, this is expressed as follows:

$$\rho_{sG} \sim \rho_{sS} \sim \rho/t_{CoSi2}, \quad (1)$$

where ρ is the resistivity of silicide.

t_{CoSi2} dependence of ρ_c, the contact resistivity, shown in Fig. 3(a) exhibits different behavior between n- and p-MOSFET. This is explained by the doping profile. Since arsenic junction has a box shape profile, ρ_c of n-MOSFET has small dependence on t_{CoSi2}. On the contrary, ρ_c of p-MOSFET is calculated to be proportional to the square of t_{CoSi2}, by assuming tunneling current process and that boron profile shown in Fig. 3(b) is expressed by Gaussian profile:

$$N \sim A_1 \exp[-t_{CoSi2}^2/A_2] \sim A_1(1-t_{CoSi2}^2/A_2), \quad (2)$$

$$\rho_c \sim \exp[A_3/N^{1/2}] \propto t_{CoSi2}^2+\alpha, \quad (3)$$

where N is concentration of dopant.

3. CMOS Performance Model

Based on the relationship between the electrical parameters and silicide thickness, CMOS propagation delay time, τ_{pd} is modeled. Firstly, the effect of ρ_c on τ_{pd} is evaluated, which corresponds to narrow channel device. τ_{pd} is expressed as:

$$\tau_{pd} \propto C_L V_{dd}(1/I_{dsatn}+1/I_{dsatp}) = C_L(R_{chn}+R_{paran}+R_{chp}+R_{parap}), \quad (4)$$

where R_{ch} is intrinsic channel resistance, and R_{para} is parasitic resistance of source/drain and is expressed as ρ_c/WX [1][2]. By using eq. (3), eq. (4) is transferred to:

$$\tau_{pd} \propto \rho_c L\varepsilon_{ox}/Xt_{ox}+\beta = A(L\varepsilon_{ox}/Xt_{ox})(t_{CoSi2}^2+\gamma), \quad (5)$$

where β and γ are terms dependent on intrinsic MOSFET parameters.

When the channel width is increased, gate wiring delay should be taken into account. Increase in τ_{pd} due to the gate RC delay is expressed as:

$$\Delta\tau_{pd} \sim R_g C_g/k = \rho_{sG} W^2 \varepsilon_{ox}/kt_{ox} = (\rho\varepsilon_{ox}/kt_{ox})(W^2/t_{CoSi2}), \quad (6)$$

where k is estimated to be 3 [3]. Therefore, total propagation delay is expressed as:

$$\tau_{pdtot} = \tau_{pd}+\Delta\tau_{pd} = A(L\varepsilon_{ox}/Xt_{ox})(t_{CoSi2}^2+\gamma)+(\rho\varepsilon_{ox}/kt_{ox})(W^2/t_{CoSi2}). \quad (7)$$

Experimental results of τ_{pd} on silicide thickness are shown in Fig. 4. Significant degradation in τ_{pd} in larger W region is due to gate wiring RC delay which is suppressed with increasing t_{CoSi2}. The channel width dependence is found to be quantitatively described with the second term of eq. (7) with k = 3. With decreasing W, τ_{pd} is improved rapidly for thin t_{CoSi2} case and the crossover of t_{CoSi2} dependence is observed. At 4.25 μm, τ_{pd} is fastest for t_{CoSi2} = 32.3 nm, where the contact resistance is dominant parasitic cause of the delay.

4. Optimization

From the above discussion, MOSFET with smaller channel width W or division into multi-finger structure is desirable to achieve high performance. It means, however, increase in design complexity and degradation of layout efficiency. In addition, silicide thickness t_{CoSi2} should also be limited in proper range from the device/process point of view. Therefore, scheme and procedure of optimization of these parameters is required. Based on eq. (7), such a scheme is proposed.

Figure 5 shows contour line of τ_{pdtot} on t_{CoSi2}-W plane for CMOS inverter (F/O=1). From SALICIDE process limitation, available t_{CoSi2} range is limited between the displayed vertical lines. Each contour line of τ_{pdtot} peaks at some t_{CoSi2} which indicates the optimum t_{CoSi2} for the corresponding channel width. Dashed line indicates optimized combination of channel width and t_{CoSi2}. Once the maximum channel or finger width is selected from the layout design consideration, t_{CoSi2} should be determined by the dashed line in Fig. 5.

5. Conclusion

A simple model regarding the impact of SALICIDE parameters on CMOS performance is presented. By using this model, the design parameter of SALICIDE process and layout design of CMOS can be prospectively attained.

References

[1] D. B. Scott et al.: IEEE Trans. Electron Devices ED-**29** (1982) 651.
[2] Y. Taur et al.: IEEE Trans. Electron Devices ED-**34** (1987) 575.
[3] A. Azuma: private communication.

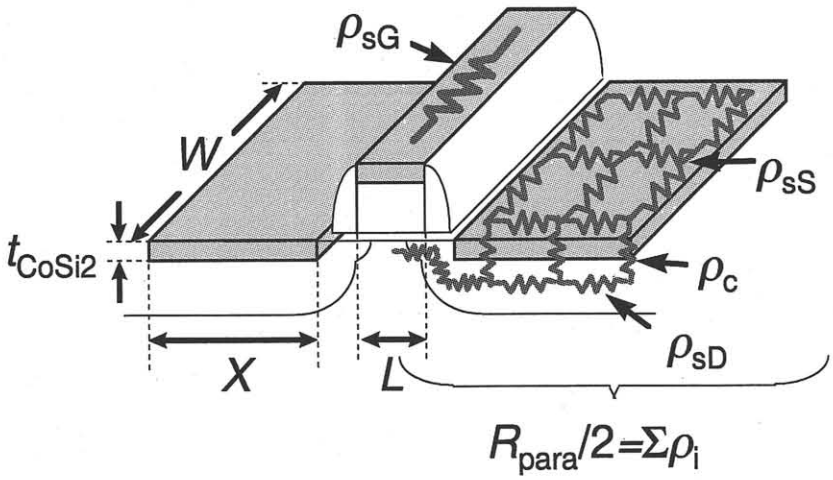

Fig. 1. Schematic diagram of parasitic resistance of salicided MOSFET and physical lengths significant for electrical properties.

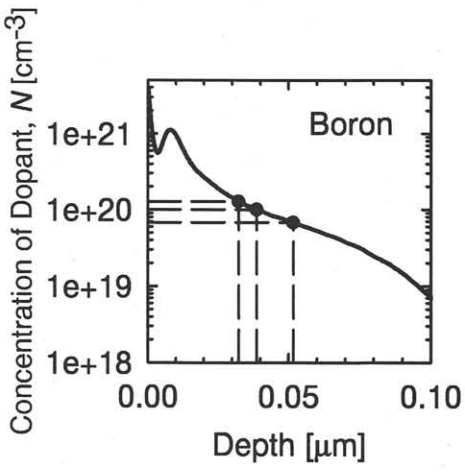

Fig. 3(b). Depth profile of Boron atoms by SIMS. Closed circles indicate $CoSi_2$/Si interfaces. Dashed lines indicate t_{CoSi2}, silicide thickness, and corresponding N, dopant concentration.

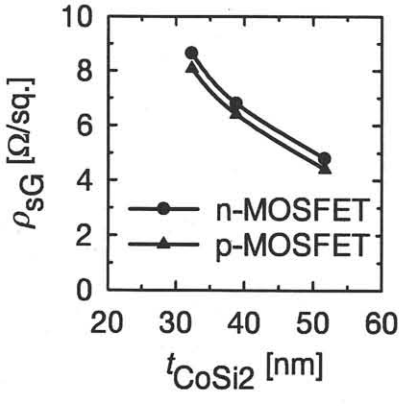

Fig. 2(a). Dependence of sheet resistivity of gate electrodes on silicide thickness.

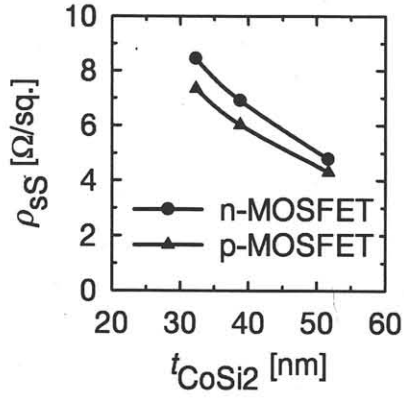

Fig. 2(b). Dependence of sheet resistivity of source/drain electrodes on silicide thickness.

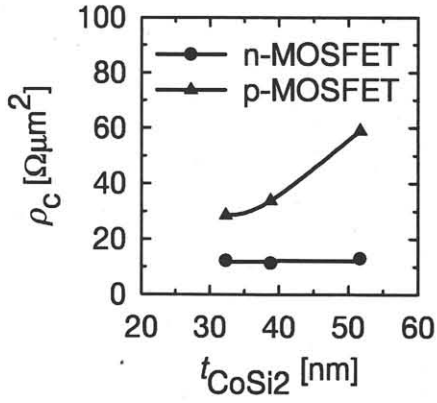

Fig. 3(a). Dependence of specific contact resistivity of $CoSi_2$/Si interface on silicide thickness.

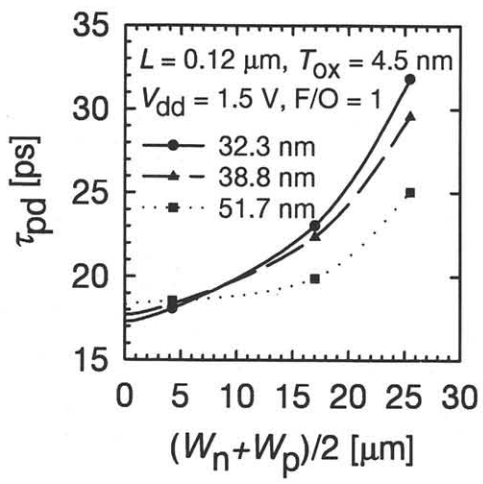

Fig. 4. CMOS propagation delay vs. channel width for three different thickness of silicide layer. In larger W region, τ_{pd} is improved with increasing silicide thickness, while, in smaller W region, τ_{pd} is degraded due to increase of contact resistance.

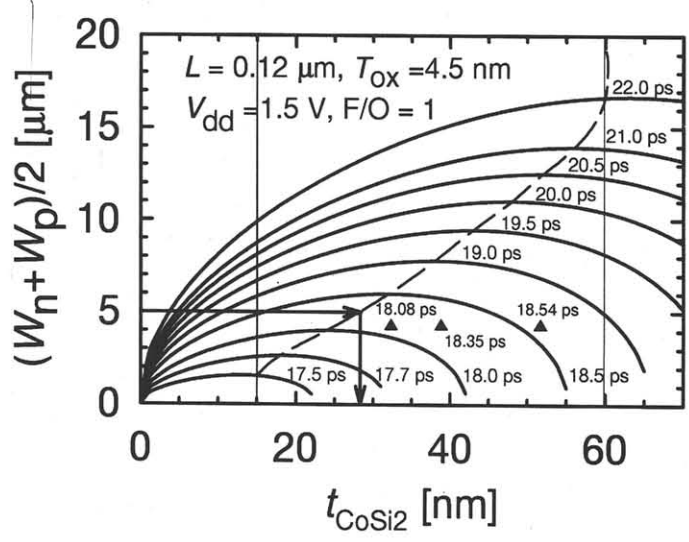

Fig. 5. Contour line of τ_{pdtot} on t_{CoSi2}-W plane for CMOS inverter (F/O=1). Symbols show measured data. Dashed line indicates optimized combination of channel width and t_{CoSi2}. Once channel width is determined, t_{CoSi2} should be selected on dotted line.