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New Stand-By Degradation Mode in n-MOSFET's with Thin Gate Oxide

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1. Introduction

In recent years there has been a growing interest in the limit to device scaling with thin gate oxide, and several investigation on this issue have been described in the literature including reliability issue[1-5].

We investigated a new degradation mode in n-channel MOSFET's (n-MOSFET's) with thin gate oxide. Drain voltage was found to cause transconductance (G_m) degradation while the gate, source, and substrate were connected to ground just as a stand-by condition. This degradation mode may be a serious problem since supply voltage is always applied to the drain of n-MOSFET's on stand-by in real LSI circuits, and has a possibility to limit the device scaling with thin gate oxide from the point of reliability as described in the present article.

2. Experimental

Conventional n-MOSFET's were fabricated on p-type Si(100) substrates. After processes of isolation and implantation for threshold voltage control, gate oxides of 3.2, 3.6, and 4.0 nm in thickness were formed at 850℃ in diluted wet O_2 ambient, followed by the gate electrode formation with WSi_x/n^+ polycrystalline Si (poly-Si). Subsequently, As^+ ions were implanted for the shallow extensions, and were also implanted for the source/drain active layer after oxide side wall formation.

As a stress bias, 3.0 to 4.0 V were applied to the drain for 9000 sec, while the gate, source, and substrate were connected to ground. This is an accelerated condition for n-MOSFET's on stand-by in real LSI circuits.

3. Results and Discussion

Figure 1 shows the stress time dependence of G_m degradation for the n-MOSFET with 0.19 μm in gate length and 3.2 nm in gate oxide thickness. G_m degradation has a power correlation to the stress time, which is the same tendency to that of hot-carrier stress. The degradation can be thought to be the results of the trap generation at the interface due to the stress and leakage current at the gate-drain overlap region. Assuming linear relationship between reciprocal of applied drain voltage and logarithm of stress time (0.9999 in correlation coefficient), the critical voltage which yields 10% degradation of G_m at 10 years can be calculated to 2.3 V from the relationship. On the other hand, the shift of the threshold voltage was less than 0.01 V via the stress, which can be ignored for the device performance as an accelerating test.

Figure 2 shows the relationship between G_m degradation and gate length for the drain voltage of 3.5 and 4.0 V. The gate oxide thickness is 3.2 nm. The degradation increases for shorter gate length, since the ratio of the damaged area in gate-drain overlap region to the gate length is higher. From the stress time dependence of G_m degradation with various stress conditions, the critical voltage which yields 10% degradation of G_m at 10 years can be calculated as described above for each gate length as shown in Fig. 3. The critical voltage decreases linearly with decreasing the gate length. From the relationship, it can be predicted that the critical voltage of 2.0 V corresponds to 0.11 μm in gate length. This is a possible case in real LSI's of 0.18 μm generation since the gate length of this generation is thought to be within 0.12 to 0.18 μm in general.

Figure 4 shows the relationship between G_m degradation and the gate oxide thickness for 0.19 and 0.26 μm in gate length. The G_m degradation becomes remarkable when the gate oxide thickness reduced to nearly 3 nm, where main current transport in the gate oxide changes from Fowler-Nordheim type to direct tunneling. This tendency for the oxide thickness is opposite to the hot-carrier degradation [3]. The thickness dependence of the degradation is thought to come from the difference of the electric field at the gate edge, but this may be also attributed to the increase of the initial, and stress induced leakage current [7] at the gate-drain

overlap region. These results suggest that the degradation will be more significant for thinner gate oxide when the device dimension becomes smaller.

From the discussion described above, G_m degradation on stand-by in n-MOSFET's has a possibility to limit the device scaling with thin gate oxide. Furthermore, this measurement can be a method to estimate thin oxide reliability, since it becomes more difficult to detect damages by conventional method for thinner oxide.

4. Conclusions

As a new degradation mode in n-MOSFET's with thin gate oxide, drain voltage was found to cause G_m degradation while the gate, source, and substrate were connected to ground just as a stand-by condition. G_m degradation increases for shorter gate length, and it becomes remarkable when the gate oxide thickness reduced to nearly 3 nm. This degradation mode has a possibility to limit the device scaling with thin gate oxide from the point of reliability.

References

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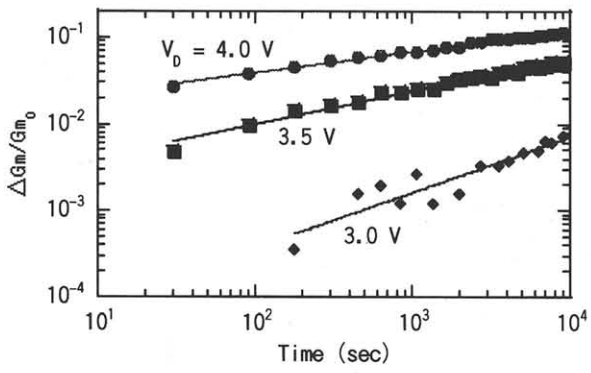

Fig.1 Stress time dependence of G_m degradation for the n-MOSFET with 0.19 μm in gate length and 3.2 nm in gate oxide thickness.

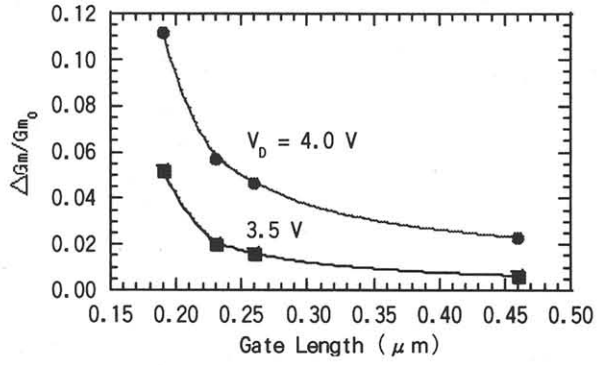

Fig. 2 Relationship between G_m degradation and gate length for the drain voltage of 3.5 and 4.0 V. The gate oxide thickness is 3.2 nm.

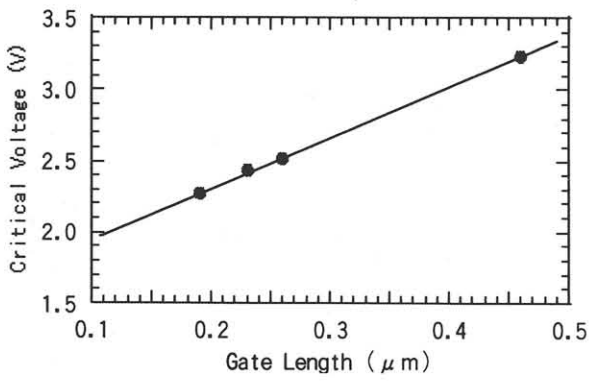

Fig.3 Critical voltage which yields 10% degradation of G_m at 10 years for the n-MOSFET's with 3.2 nm in gate oxide thickness.

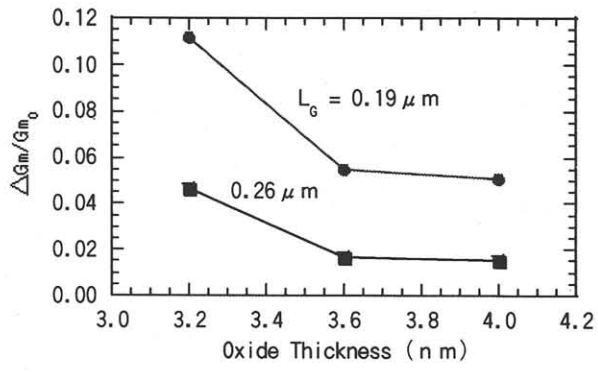

Fig. 4 Relationship between G_m degradation and the gate oxide thickness for 0.19 and 0.26 μm in gate length.