Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 142-143



# Analysis of Distortion Behavior Considering Polydepletion Effect in MOS Transistors

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## I. Introduction

As MOS transistors have been scaled down, doping concentration for polysilicon gate cannot be arbitrarily high for most technologies, so that polydepletion effect becomes important. This polydepletion effect decreases effective gate capacitance and finally degrades current drive capability and operating speed of devices [1]. Hence modeling of the polydepletion effect is essential to describe nonlinear characteristics of transistors. The goal of this work is to characterize the polydepletion effect dependence on transistor bias using a simple effective gate capacitance model without a threshold voltage shift, and to show its influence on nonlinear behavior of MOS transistors which is shown up as distortion in analog circuits.

## II. Modeling of Polydepletion Effect

### *A. Polydepletion Effective Capacitance Model*

For N-channel MOS devices with non degenerately doped polysilicon gate, a depletion layer will be formed in the polysilicon gate when positive gate bias is applied as shown in Fig.1. This polydepletion effect is well known for devices with gate oxide of about 50 Å or less, and becomes more serious as the gate oxide thickness decreases as shown in Fig.2, [1], [2]. Voltage drop across polydepletion layer can be obtained by solving Poisson's equation with the boundary condition of $\epsilon_{ox}E_{ox} = \epsilon_{si}E_{poly}$ at the interface between polysilicon and oxide. This is given by

$$V_{poly} = V_{gs} - V_{fb} - \psi_s(V_{gs}, V_{ds}) + \alpha_p \cdot \left\{1 - \sqrt{1 + \frac{2}{\alpha_P}[V_{gs} - V_{fb} - \psi_s(V_{gs}, V_{ds})]}\right\} \quad (1)$$

$$\text{where} \quad \alpha_P = \frac{q\epsilon_{si}\epsilon_o N_{poly}}{C_{ox}^2}$$

where $V_{gs}$ is gate bias with respect to the source, $V_{fb}$ is the flat band voltage, $\psi_s$ is the average surface potential in the inversion region, $C_{ox}$ is the gate oxide capacitance per unit area, and $N_{poly}$ is the polysilicon doping concentration which can be extracted from C-V measurement and device simulation. $V_{gs}$ is reduced by $V_{poly}$, and we have the effective gate voltage of $V_{gseff} = V_{gs} - V_{poly}$. Using $V_{gseff}$ with gradual channel approximation to surface potential, capacitance due to polydepletion layer can be defined as

$$C_{poly} \equiv \frac{V_{gseff}/V_{gs}}{1 - V_{gseff}/V_{gs}} C_{ox} \quad (2)$$

In Eq. (2) $V_{gseff}$ is a function of terminal voltage, so that we have bias dependent $C_{poly}$ using an approximate surface potential expression, $\psi_s$ [3]. This poly depletion capacitance is in series with the gate oxide capacitance so that overall effective gate capacitance can be written as

$$C_{oxeff} = \frac{C_{poly}C_{ox}}{C_{poly} + C_{ox}} = \frac{V_{gseff}}{V_{gs}} C_{ox} \quad (3)$$

which depends on bias, $V_{gs}$ and $V_{ds}$ through $\psi_s$.

### *B. Charge Sheet Model Including Polydepletion*

With Eq. (3), we can modify the charge sheet model current equation [4] by substituting $C_{ox}$ with $C_{oxeff}$, and compared this model with $0.3um$ MOS transistor in Fig.4. The proposed model shows good agreement with measured I-V characteristics while the model neglecting polydepletion effect overestimates drain current for high gate voltages where the polydepletion effect becomes prominent.

$$I_d = \mu C_{oxeff}\frac{W}{L}[\gamma V_t(\psi_{sL}^{1/2} - \psi_{so}^{1/2}) + (V_{gb} - V_{fb} + V_t)\cdot (\psi_{sL} - \psi_{so}) - \frac{1}{2}(\psi_{sL}^2 - \psi_{so}^2) - \frac{2}{3}\gamma(\psi_{sL}^{3/2} - \psi_{so}^{3/2})] \quad (4)$$

## III. Discussion and Results

As the polysilicon doping level increases, the proposed model becomes the same as the conventional charge sheet model as shown in Fig.4. Using Eq. (4) and power series analysis [5], intermodulation distortion current is simulated with different polysilicon doping concentration under quasi static assumption as shown in Fig.5. Since the current degradation becomes worse in the saturation region, simulated results show the differences in the second and third distortion nulling for high $V_{ds}$. This implies conductance characteristic deviates from the prediction by the conventional model as the oxide thickness decreases. Therefore, modeling of physical phenomenon associated with thin gate oxide becomes more important for analysis of distortion.

## IV. Conclusion

Polydepletion effect contribution to distortion behavior is discussed by using bias dependent effective capacitance model. The model developed here also predicts its influence on distortion behavior of transistors.

## References


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[5] S. A. Maas, *Nonlinear Microwave Circuits*, IEEE Press, New york, 1997.

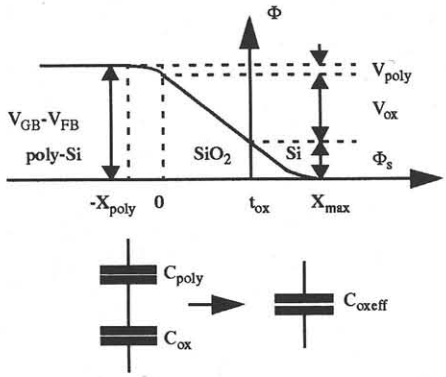




Fig.1. Schematic diagram for potential distribution for MOS gate structure and its equivalent capacitance representation

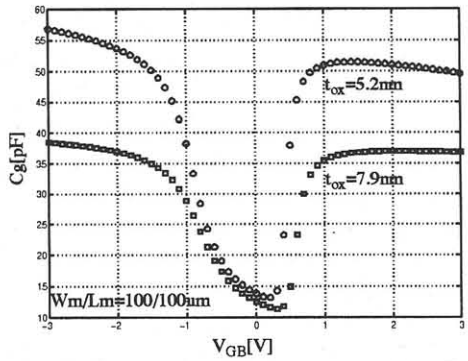



Fig.2. C-V characteristics of MOS capacitors with different gate oxide thicknesses showing poly depletion effect ($N_{poly}$=1e19/cm$^3$ extracted)

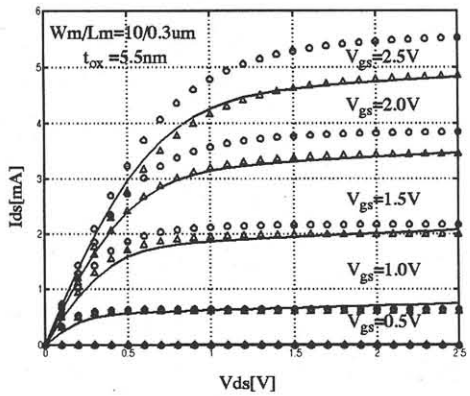



Fig.3. Current voltage characteristics for 0.3um NMOS transistor with varying gate voltages, and lines are measured data while symbols are modeled data using (4) with $N_{poly}$=1e19/cm$^3$ (triangle for model with polydepletion effect, circle for model without polydepletion effect )

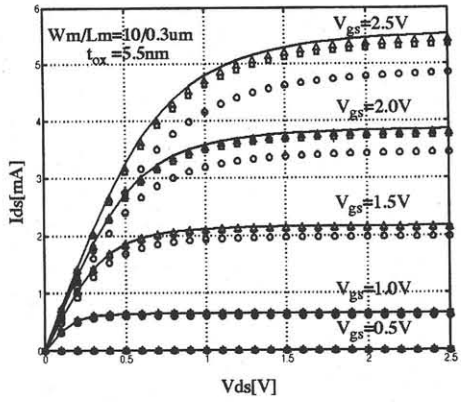
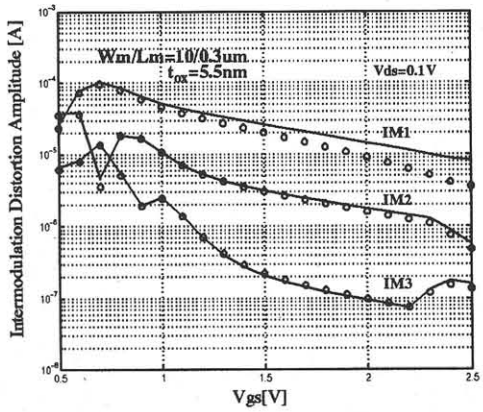
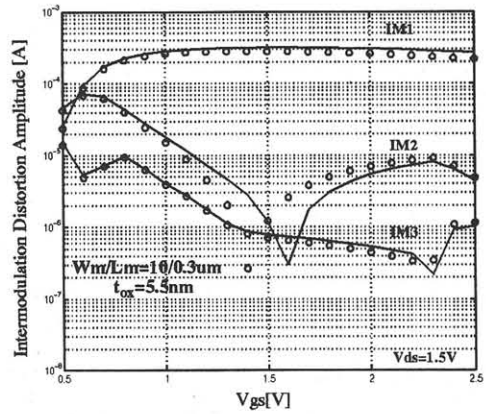



Fig.4. Comparison of current voltage characteristics of developed model with various poly silicon doping concentration. (circle for $N_{poly}$=1e19/cm$^3$, square for $N_{poly}$=5e19/cm$^3$, triangle for $N_{poly}$=9e19/cm$^3$, and line for ignoring polydepletion effect.)




a) Vds = 0.1V




b) Vds = 1.5V

Fig.5. Simulated intermodulation distortion current amplitude for triode region (Vds=0.1V) and saturation region (Vds=1.5V) . (line for $N_{poly}$=9e19/cm$^3$, circle for $N_{poly}$=1e19/cm$^3$ , and varying gate input voltages are $0.1\cos(2\pi f_1 t)$ and $0.1\cos(2\pi f_2 t)$ where $f_1$=10kHz and $f_2$=9.5kHz )