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A Novel Diffusion Resistant P-Base Region Implantation for Accumulation-Mode 4H-SiC Epi-Channel Field Effect Transistor

Rajesh Kumar, Jun Kozima, and Tsuyoshi Yamamoto
Research Laboratories, DENSO CORPORATION, Nisshin-shi, Aichi 470-0111, Japan
Tel: +81-5617-5-1084; Fax: +81-5617-5-1185; E-mail: kumar@rlab.denso.co.jp

SiC power devices are extremely promising for high power switching applications because of low power losses as compare to Si power devices. For SiC power devices, 4H-SiC polytype is an attractive candidate material for high temperature, high frequency, and high power device applications[1]. As SiC material possesses extremely high thermal, chemical, and mechanical stability upto 1300℃ because of large Si-C bond energy of ~5.0eV. It is not feasible to dope SiC by thermal diffusion as is commonly used for Si device processing. Instead, dopants are introduced by ion implantation at elevated temperatures. Group-IIIA atoms, viz., B, Al, and Ga are usually employed as p-type dopants in SiC. In 4H-SiC, the Al shallow acceptor energy level is at E_V+(191~230meV). The B-related shallow and deep levels are at E_V+(285~390meV) and E_V+(540~720meV), respectively. The B atoms provide an advantage that it can be implanted deeper into the SiC than the other group-IIIA impurities for a given implantation energy and causes less implantation damage to the SiC crystal lattice. However, long B diffusion tail has been observed in SiC polytypes[2]. Chilukuri et al.[3] have also reported the B diffusion in the fabricated 4H-SiC ACCUFET. The B diffusion from the p-base region resulted in the inversion of n-type accumulation channel surface to p-type, and hence the formation of an inversion channel. Usually, high power applications require a high level of unit-cell integration, which can be achieved by reducing the pitch of unit-cell. However, B diffusion can limit the reduction of p-base spacing of unit-cell due to increasing JFET pinch resistance. Earlier, we reported the accumulation-mode epi-channel trench MOSFET structure for SiC power devices, named epi-channel field effect transistor (ECFET)[4]. In this work, we employ a novel implantation technique using the C/B sequential implantation to control the B lateral and vertical diffusion from the p-base region of the planar 4H-SiC ECFET.

The schematic cross-section of the fabricated planar 4H-SiC ECFET device is shown in Fig.1. Multiple energy box profile for C/B sequential implantation, simulated with SUPREM (TMA), is used to achieve a p-base region with a junction depth of ~ 0.75μm. The B mean doping concentrations in the implanted region was ~$1x10^{18}cm^{-3}$. The C concentration was varied from $1.0x10^{16}cm^{-3}$ to $1.0x10^{20}cm^{-3}$. All implantations were performed at 1000℃ to prevent amorphization, thereby limits the implantation induced damages. Two striking phenomenons were observed in SIMS profiles as shown in Fig.2. (i) A long B diffusion tail of more than 1μm was observed, and (ii) The B diffusion tail is almost suppressed when the sequentially implanted C atoms concentration reaches about $1.0x10^{19}cm^{-3}$. The sequentially implanted C prior to the B ion implantation creates a C-rich region containing both Si- and C-vacancies. It is likely that excess Si-vacancies increase the probability for the B atom to occupy the Si-lattice site and hence trap B atoms to limit their diffusion. The B atom residing at Si-lattice site forms the shallow acceptor level[5]. We performed the current deep level transient spectroscopy (*i*-DLTS) measurements to establish the inter-correlation between the B diffusion and the electrically active defects introduced by the C/B sequential implantation. It was found that the formation of deep defect level is also completely suppressed for the same ratio (C:B=10:1) as that for the B diffusion in 4H-SiC (Table-1). In this way, C/B sequential implantation also improves the electrical activation of B shallow acceptors. The I_{DS}-V_{DS} characteristics of fabricated accumulation-mode planar 4H-SiC ECFET devices at room temperature are shown in Fig.3. The effectiveness of C/B sequential implantation in suppressing the JFET pinch effect is clearly visible from the 3~4 fold increase in I_{DS} of ECFET with sequentially implanted p-base region which was scaled down to a spacing of 3μm. 2D numerical device simulations also predict a lower voltage drop in the JFET region of the ECFET. Therefore, this novel implantation technique open doors for the larger packing densities through unit-cell pitch reduction for SiC high power device applications.

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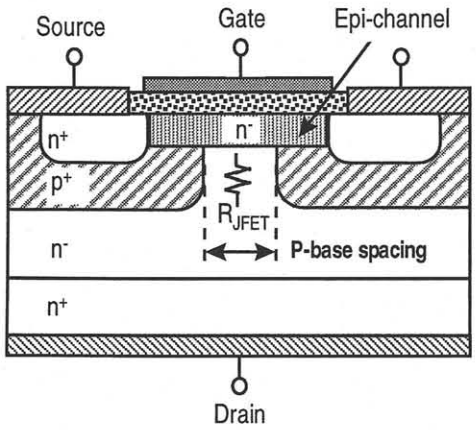

Fig.1 Schematic structure of accumulation-mode planar epi-channel field effect transistor (ECFET).

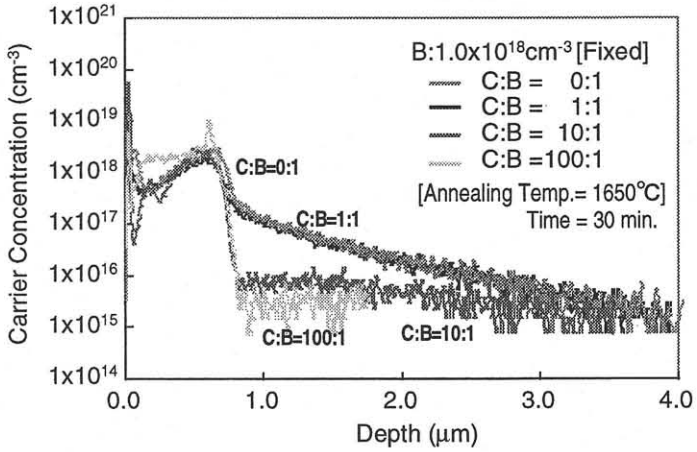

Fig.2 SIMS profile of B implanted 4H-SiC showing a long diffusion tail after annealing at 1650°C for 30min. in Ar ambient. The C/B sequential implantation limits the B diffusion in 4H-SiC.

Table 1: Parameters derived from the current deep level transient spectroscopy (*i*-DLTS) analysis of C/B sequentially implanted 4H-SiC.

Sample	Peak Temperature	Defect	Ionization Energy (Δ E)	Deep Defect Density (N_T)
B1 (C:B=0:1)	285K	D-center	529.0meV	$9.4x10^{18}cm^{-3}$
CB2 (C:B=0.1:1)	285K	D-center	566.0meV	$2.3x10^{18}cm^{-3}$
CB3 (C:B=1:1)	285K	D center	586.0meV	$9.9x10^{17}cm^{-3}$
CB4 (C:B=10:1)	-	D center	-	-
CB5 (C:B=100:1)	-	D center	-	-

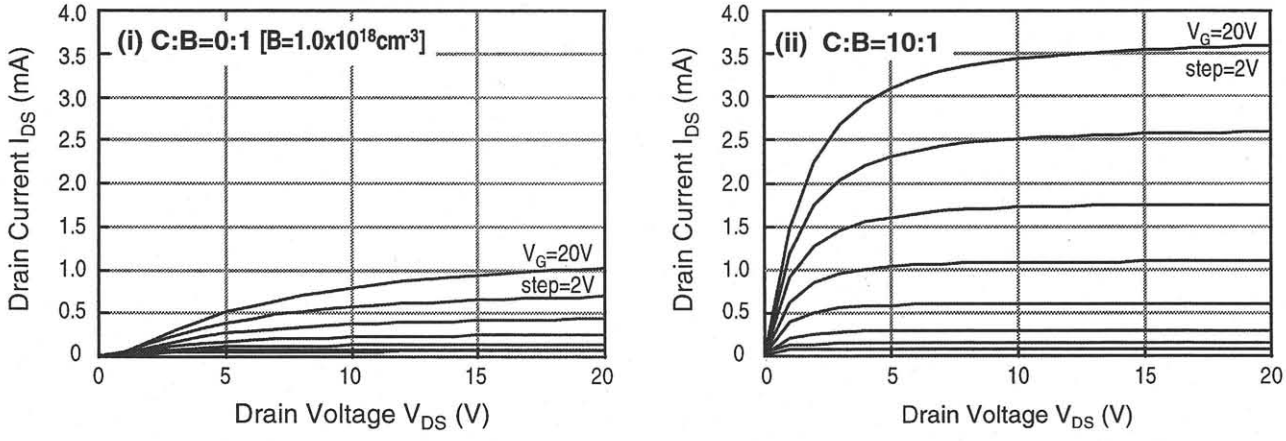

Fig.4 I_{DS}-V_{DS} characteristics of accumulation-mode planar 4H-SiC ECFET with (i). B implanted p-base region, and (ii). C/B sequentially implanted p-base region. The effectiveness of C/B sequential implantation in suppressing the JFET pinch effect is clearly visible from the 3~4 fold increase in I_{DS} of planar ECFET (P-base spacing= 3μm).