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Failure Analysis of Chip Interconnects Using Picosecond Imaging Circuit Analysis

J. A. Kash, Dan Knebel, and J. C. Tsang

IBM Thomas J. Watson Research Center, P.O. Box 218
Yorktown Heights, NY 10598, USA
phone: 914-945-1448 Fax: 914-945-2141 Email: jeffkash@us.ibm.com

1. Introduction

While tools exist which measure electrical waveforms in older chips, their operation depends on the availability of direct access As the number of layers of metallization in modern ICs have grown so that the lower layers are completely covered, and as "flip-chip" packaging has become widely used, direct physical access to the metal lines carrying the electrical signals has become very difficult to obtain. As a result, measuring the signals on the lines by mechanical probe tips or electron beams is no longer possible [1]. Picosecond Imaging Circuit Analysis (PICA) [2,3] is a new optical imaging method for measuring the electrical switching activity in CMOS integrated circuits through the backside of the substrate. PICA measurements do not require access to the metal lines. Here we describe the use of PICA to localize chip interconnect failures.

2. Light Emission from Silicon FETs

While silicon is opaque in the visible, it is reasonably transparent at infrared wavelengths, even when doped. As a result, optical methods at wavelengths near 1 micron can be used to measure circuits and devices through the backside, especially when the substrates are thinned to 200 microns or less. Although silicon is an inefficient emitter of light, it is known that modern silicon FET's emit small but detectable amounts of light when they are in saturation. This emission is not due to normal interband recombination but arises instead from intraconduction and intravalence band transitions of carriers with high kinetic energies.

3. The PICA Technique

Because of the complementary character of CMOS gates, in the absence of switching activity no current passes through CMOS gates, and there is no hot carrier light emission. However, when CMOS gates switch states, there is current flow, and the transient current pulses due to the switching produce temporally coincident light emission. If the light pulses are measured by single photon counting detectors, it is possible to time resolve the emission with a full width at half maximum of less than 100 psec, and to measure time delays between emission peaks to better than 30 psec [2]. As with any optical technique working at wavelengths near 1 micron, individual light emitting gates can be individually distinguished on the 0.5 micron scale by conventional optics.

Elementary analysis of the switching induced luminescence provides a wide variety of information about device and circuit performance. These include the separation of the dynamic behavior of nFETs and pFETs, the identification of the direction of switching transitions from either ground to power supply or supply to ground, gate-to-gate delays, as well as various kinds of switching anomalies [3,4].

4. Failure Analysis of Chip Interconnects

A common failure of chip interconnects is an overly resistive metal line or via. In extreme cases, the downstream logic gates will not switch at all, which can be observed by a complete lack of emission. Often, however, the resistance will be small enough that the circuits may still function partially, but with substantially increased switching delays. The result may be a chip which functions at low clock frequencies but not at required high frequencies.

An example of using PICA to locate this type of wiring defect comes from a yield learning cycle of a recent CMOS process. Module level testing of a microprocessor revealed timing related failures. Root-cause analysis was performed on selected samples to determine sources of the timing failures, and diagnostics generated from at-speed electrical testing were used to predict possibly faulty circuit elements. A sample with a timing related failure in a register file was selected for detailed PICA analysis.

The probable fault location in the register file had been isolated using software diagnostics to a particular latch pair, which could be stimulated repeatedly at high frequency. A portion of the schematic diagram is shown in Figure 1.

A simulation of the defect-free circuit was made to predict both the static emission pattern of the register file and a time-resolved emission waveform for a latch pair. Light emission pulses are expected to be emitted synchronously with the peaks in the current waveform of the simulation.

Figure 2 is a time-integrated emission pattern from the register file in the region of the faulty latch pair. Two latch pairs are circled. One of the pairs appears identical to all the others in the register file. The other circle evidently contains the faulty latch pair. The time-resolved PICA optical waveforms for both of the circled latch pairs are plotted in figure 3. Each optical waveform represents emission intensity vs. time for all of the transistors in the latch pair.

For the good latch pair, the occurrence times of the emission spikes compared favorably with the predicted

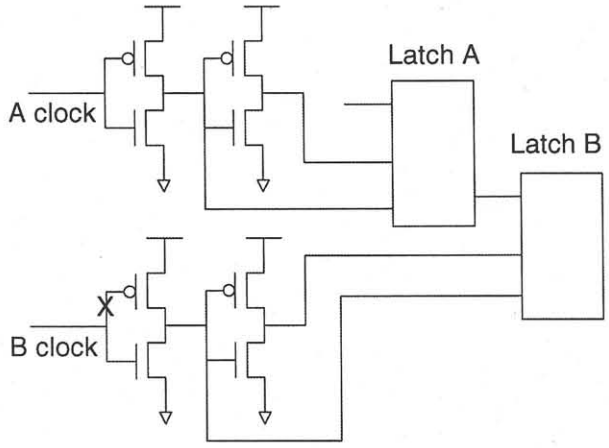

Fig. 1 Schematic of a latch pair in the faulty register file. The location of the defective metal interconnect is marked with an X.

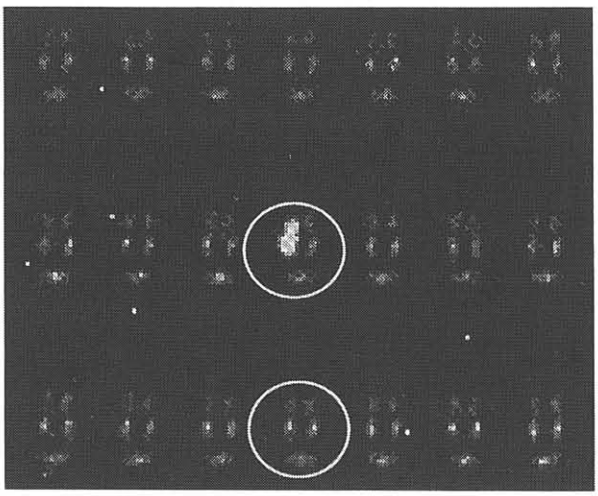

Fig. 2 Time-integrated emmision from a portion of the register file. The faulty latch pair and a normal latch pair are circled.

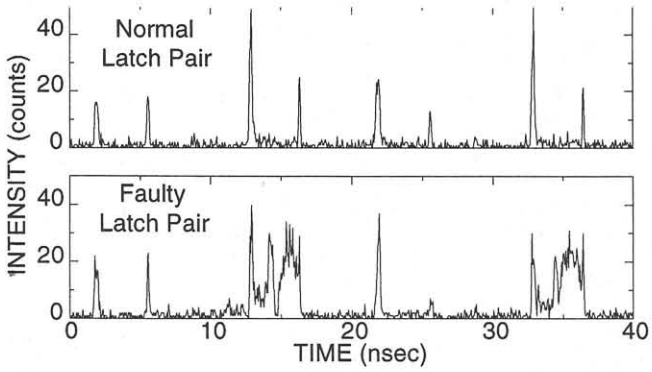

Fig. 3 Optical waveforms from a normal and the faulty latch pairs, (circled in fig. 2). The A clock is active from 2 to 5.5 nsec and from 22-25.5 nsec. The B clock is active from 13 to 16.5 nsec and from 33 to 36.5 nsec. The latches are storing a zero in the first half of the waveforms, and a one in the second half.

emission pattern, coinciding with the launch and capture times determined by the rising and falling edges of the clocks.

The time-resolved emission waveform of the faulty latch pair shows that the circuit was correctly identified as the source of the failure. Information extracted from the emission waveform was used to verify the anticipated additional delay due to the defect. The excess emission is seen to occur only when the B clock is active (high). In addition, the excess emission occurs in all clock cycles, regardless of whether the latch pair is storing a zero or a one. This ability to correlate emission data with circuit timing is a critical element that sets PICA apart from static-emission analysis.

Of the suspected defect types and locations, only one could produce these time-resolved emission waveforms: a series resistance between the B clock input and the pull-up of the first inverter in the circuit. The location of this resistance is indicated by the X in figure 1. A simulated PICA waveform of the circuit containing the defect matches the signature of the measured optical waveform. A PICA measurement using a higher power objective would have been able individually spatially resolve the malfunctioning transistor, but the time-resolved data had already pinpointed the location of the failure. As determined by scanning-electron microscope images, the defect was indeed identified at the suspected location.

5. Conclusions

PICA is a fully noninvasive method for measuring switching activity in CMOS ICs. It is capable of detecting switching activity through the backside or frontside of a chip with picosecond temporal resolution. Spatial and temporal data for numerous transistors is gathered in a single image and can be stored for off-line analysis making PICA a highly productive analytical tool. We have shown its use here in diagnosing an interconnect that caused a timing-only defect. PICA may also be applied to many other tyes of defects.

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