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Device Design Considerations for Sub-50 nm CMOS

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Abstract

SOI MOSFETs are considered to be the most viable structures for sub-50 nm CMOS. This paper discusses various device design and process considerations for single-gate and double-gate thin-body SOI MOSFETs.

Introduction

As MOSFET devices are scaled down to gate lengths of 50 nm and beyond for improved density and performance, the requirements for body-doping concentration, gate-oxide thickness, and source/drain doping profiles to control short-channel effects become increasingly difficult to meet when conventional bulk-Si structures are employed. An alternative approach to controlling short-channel effects MOSFETs is to use an extremely thin (<10 nm) silicon film to eliminate subsurface leakage paths [1]. The most effective approach is to use a double-gate MOSFET, which provides much higher current for a given silicon area as well as superior short-channel behavior [2]; the fabrication of a double-gate MOSFET with perfectly aligned gate electrodes presents greater processing challenges, however. This paper discusses design and process considerations for sub-50 nm thin-body silicon-on-insulator (SOI) and double-gate MOSFETs.

Thin-Body MOSFET

A schematic cross-sectional view of a thin-body MOSFET is shown in Fig. 1. The use of an ultra-thin channel eliminates the requirement for very high body-doping concentrations to control short-channel effects. If a low doping concentration ($<10^{17}$ cm^{-3}) is used, the body depletion charge contributes negligibly to the threshold voltage, so that threshold-voltage variation due to dopant fluctuations [3] is eliminated. In order to reduce parasitic series resistance, the silicon film thickness is increased in the source and drain (S/D) contact regions to create a recessed-channel structure [4]. Design studies of 25 nm thin-body MOSFETs were conducted using Silvaco ATHENA and ATLAS 2D process and device simulations [5]. Fig. 2 shows the plot of I_{ds} vs. V_{gs} for V_{ds}=1V for body thicknesses ranging from 2.5 nm to 10 nm, indicating that a body thickness of ~5 nm provides the best tradeoff between high drive current and low leakage current (<10 nA/μm). A mid-gap work-function gate provides symmetric CMOS threshold voltages (Fig. 3).

A difficulty associated with the fabrication of thin-body MOSFETs is the formation of the channel film. If etch-back or oxidation-thinning processes are employed, the uniformity of the body thickness will be limited by the uniformity of the starting SOI layer. Formation by thin-film deposition is advantageous for achieving better thin-body thickness uniformity. Thin-body SOI MOSFETs have been successfully fabricated in deposited and laterally crystallized amorphous Si (a-Si) [6]. Good short-channel behavior was demonstrated (Fig. 4), validating the thin-body MOSFET approach.

Double-Gate MOSFET

The primary challenge in fabricating a double-gate MOSFET is to obtain two gates which are self-aligned to each other and to the S/D regions. The SOI "gate-all-around" transistor was the first high-performance double-gate MOSFET to be successfully demonstrated [7]. This device is susceptible to edge leakage problems, however [8], and suffers from significant parasitic gate capacitance because the gate material underneath the Si in the S/D contact regions cannot be completely removed by the gate etch. An alternative approach is to fabricate a vertical double-gate MOSFET. The "folded-channel" MOSFET has recently been demonstrated to be a promising structure for achieving transistors with gate lengths down to 30 nm, with excellent turn-off characteristics (Fig. 5) and short-channel behavior (Fig. 6).

Summary

In summary, the thin-body MOSFET is a promising approach to achieving sub-50 nm gate-length CMOS devices which are immune to channel-dopant fluctuation effects. The gate oxide need not be inordinately thin (2 nm) to achieve reasonable drive current (650 μA/μm) and acceptable off current (8 nA/μm), and a single gate material can be used to achieve symmetric threshold voltages for n- and p-channel MOSFETs. Because the performance of a thin-body MOSFET is highly dependent on body thickness, channel formation by thin-film a-Si deposition and subsequent solid-phase epitaxial crystallization is preferred over etch-back or thinning techniques. The double-gate MOSFET is the most promising structure for CMOS devices scaled to the ultimate limit of 20 nm. Its primary drawback is its higher fabrication process complexity, needed in order to attain self-aligned gates with low parasitic gate capacitance and S/D series resistance.

Acknowledgement

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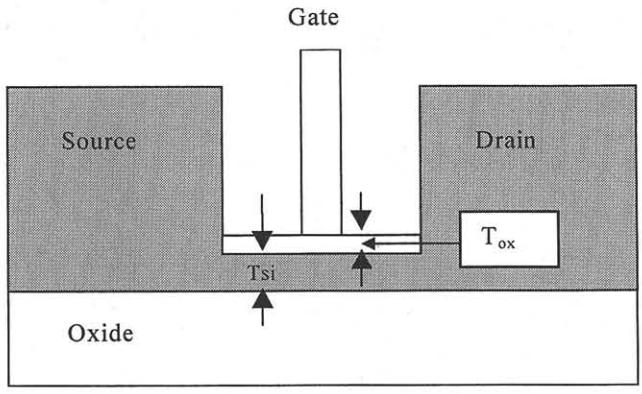

Figure 1: Thin-body MOSFET structure.

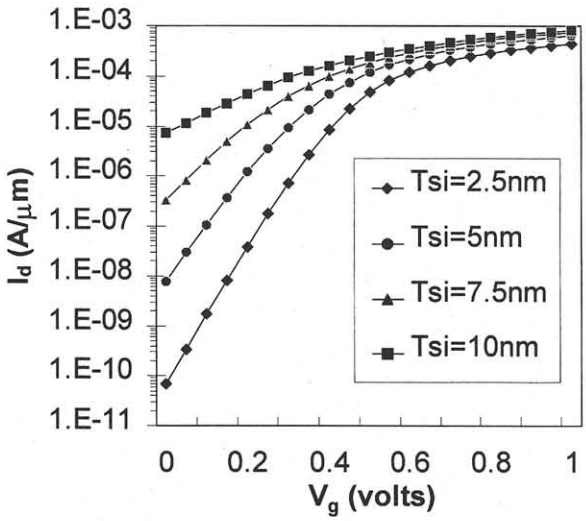

Figure 2: Simulated 25 nm gate-length thin-body MOSFET transfer characteristics for various body thicknesses [5]. $N_{body} = 10^{16}$ cm^{-3}; $T_{ox} = 2$ nm; $\Phi_M = 4.74$ V.

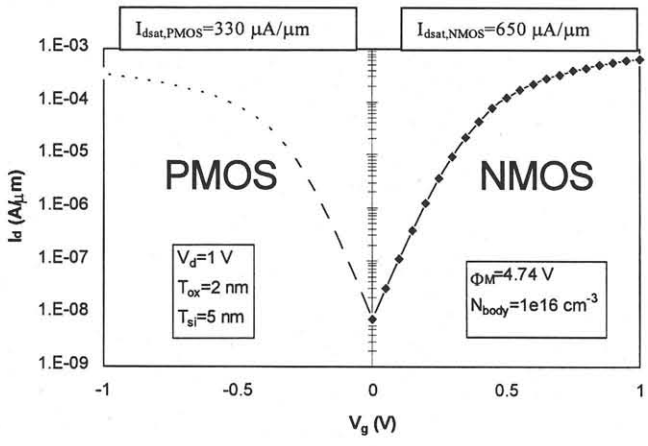

Figure 3: Simulated transfer characteristics for optimized 25 nm gate-length thin-body MOSFETs [5].

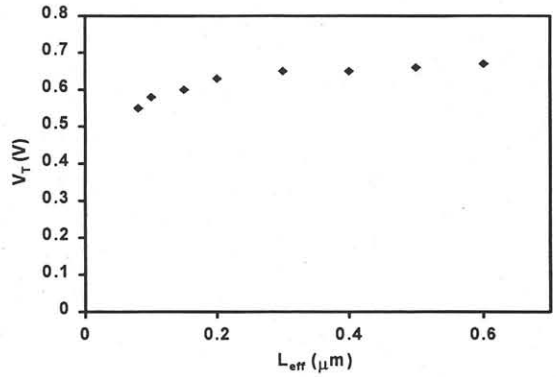

Figure 4: Threshold voltage roll-off for fabricated thin-body MOSFETs [6]. Channel (20 nm thick) was formed by deposition of a-Si and subsequent lateral epitaxial crystallization.

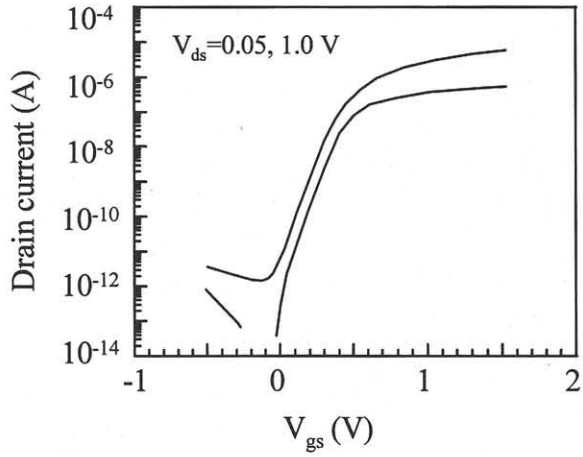

Figure 5: Transfer characteristics for fabricated double-gate MOSFET [9]. $L_{gate} = 30$ nm; T_{Si}=20 nm.

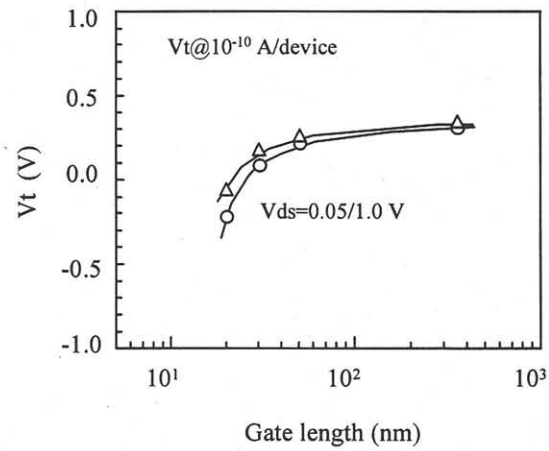

Figure 6: Threshold voltage roll-off for fabricated double-gate MOSFETs [9]. T_{Si}=20 nm.