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Dependence of Sub-Threshold Hump and RNWE Characteristics on the Gate Length by TED

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***Abstract*— We, for the first time, have shown that sub-threshold hump and RNWE characteristics strongly depend on the gate length and the mechanism is well explained by the transient enhanced diffusion (TED) due to S/D implant damage. It was also found that a degree of hump strength with gate length shows a maximum point where the threshold voltage is highest.**

I. Introduction

As the devices are scaled down, for a highly integrated circuit, a shallow trench isolation (STI) is indispensable. However, STI has been accompanied by severe problems such as the reverse narrow width effect (RNWE) and sub-threshold hump (hump) in N-MOSFET's, which are caused by crowding of gate fringing field at STI-corner [1]-[3].

In this paper, we, for the first time, found that the sub-threshold hump and RNWE characteristics depend on the gate length and the mechanism is well explained by the transient enhanced diffusion (TED) due to S/D implant damage. It was also found that a degree of hump strength with gate length shows a maximum point where the threshold voltage is highest.

II. Experimental and Results

The process used in this work is a 0.2μm CMOS process. A typical STI process was performed for isolation (Fig.1). A WNx/poly stacked file was used for a gate film. After S/D LDD, RTA was applied for activation. We prepared two representative samples for NMOS, which are a sample A with a boron halo(arsenic NM), and a sample B without a boron halo (phosphorus NM). Fig.2 shows the sub-threshold hump characteristics caused by a corner transistor of STI. It can be seen that the strength of the hump varies as the gate length. The hump is strongest at the gate-lengths of 0.25μm and 0.5μm, at which the threshold voltage is highest, for sample A and sample B, respectively (Fig.3). At longer gate-length, the strength of the hump characteristics is remarkably reduced. The hump can not be seen at the gate-length of 10μm. The threshold voltage of the main transistor and STI corner transistor is shown in Fig.4, which are measured at the drain current of 1μA/(W/L=1μm) and 10nA/(W/L=1μm), respectively. The figure shows that the threshold voltage difference between the main transistor and the corner transistor which represents a degree of strength of the hump and RNWE characteristics is also highest at the gate length of 0.5μm and also lowest at the gate length of 10μm. Fig.5 shows the RNWE for the sample B. The RNWE at the short gate length is stronger than that at the long gate-length like the hump characteristics.

III. Simulation and Discussion

The point to explain the dependence of RNWE and hump on the gate-length is that the boron depletion near STI gets higher at short gate-length than long gate-length. Because the boron depletion or pile-up is enhanced by TED due to S/D implant damage (interstitial), a degree of the depletion or pile-up of impurity is modulated by the distance from the S/D extension or the gate-length.

The boron profile used for simulation is shown in Fig.6. The STI edge near S/D extension (point B) is affected by TED due to interstitial Si generated by S/D implant damage. On the other hand, in case of the point A, TED only takes place at the short gate-length affected by S/D implant damage (interstitial Si). So, the boron depletion near STI gets higher as the gate-length gets shorter, and it results in strong hump and RNWE characteristics at the short gate-length. The reduction of the hump characteristics at much shorter gate-length is explained by the fact that the parasitic transistor at STI-corner is less sensitive to the SCE than the main transistor [1],[2]. By using the above model the hump and RNWE was simulated using 2-D process and 3-D device simulator. Fig.7 shows the simulated results of hump and RNWE characteristics. These results explain well the gate-length dependence of the hump and RNWE.

IV. Conclusion

We, for the first time, have shown that the sub-threshold hump and RNWE characteristics depend on the gate length and these results are well explained by the transient enhanced diffusion (TED) due to S/D implant damage. It was also found that a degree of hump strength with gate length shows a maximum point where the threshold voltage is highest.

References

[1] Lex A.Akers et.al., ,IEEE ED.1987,pp2476
[2] P. Sagoity et.al, ,IEEE ED. 1996,pp.1900
[3] Atsuki Ono et.al, IEDMTech.Dig.,1997,pp.227

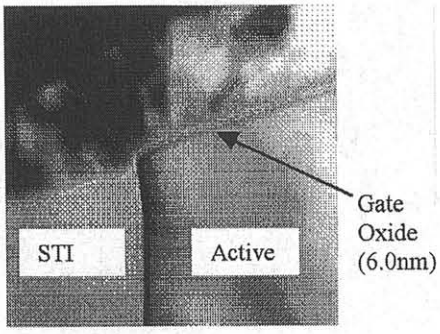


Fig.1 The cross-sectional TEM photograph of STI isolation

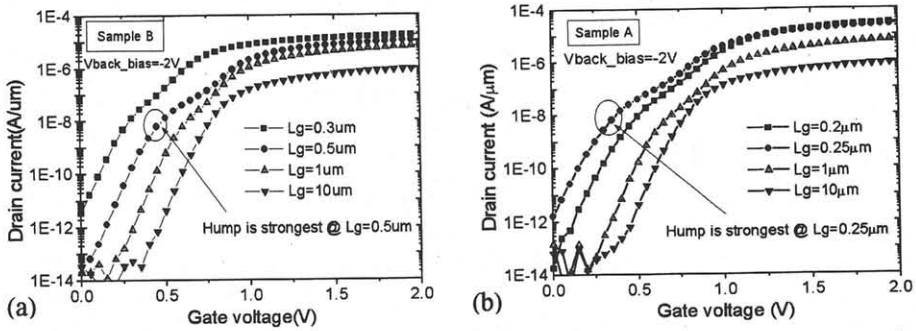


Fig.2 The hump versus the gate-length (a) sample A,(b) sample B. The hump is strongest at the gate-length of (a) 0.25μm and (b) 0.5μm, at which the threshold voltage is highest, respectively, as shown in Fig.2 .It is clearly disappeared at the gate length of 10μm.

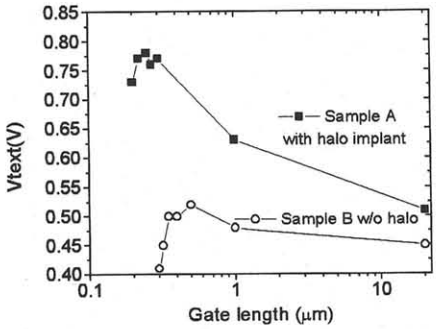


Fig.3 The reverse short channel effect (RSCE) of sample A and B. The hump is strongest at the highest threshold voltage (0.25μm and 0.5μm).

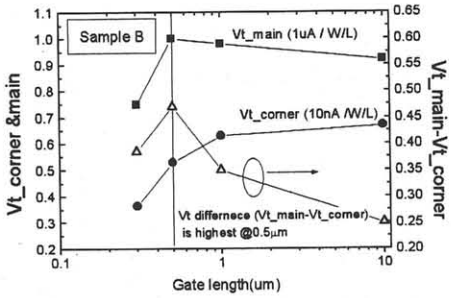


Fig.4 The threshold voltage of the main transistor and corner transistor. (Sample B). The threshold voltage difference (Vt_main – Vt_corner)is highest at 0.5μm like hump characteristics.

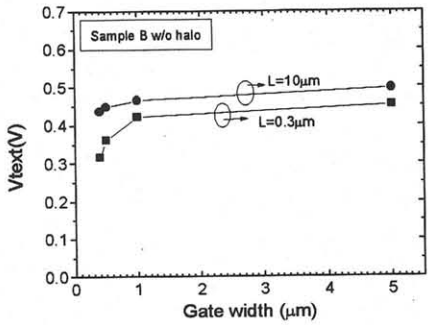
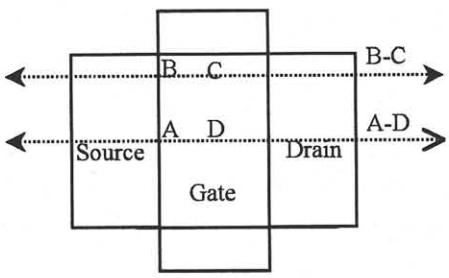


Fig.5 The RNWE (Sample B). The RNWE at the short gate-length is stronger than that at the long gate-length.



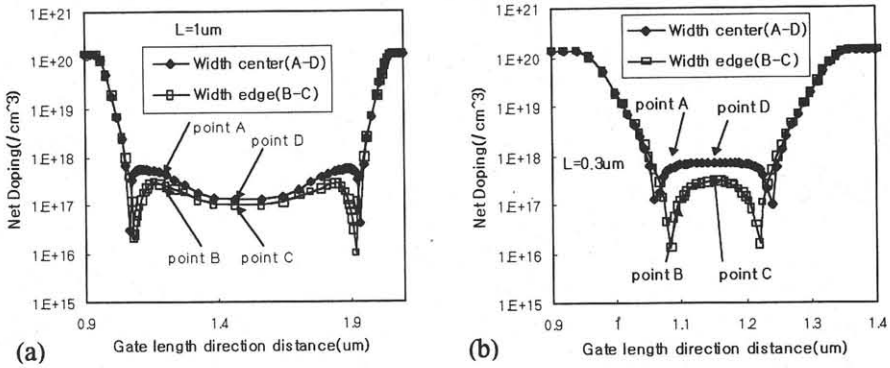


Fig.6 The boron-profile used for simulating mechanism of the hump and RNWE dependence on the gate-length. The boron depletion at the short gate length(b,L=0.3μm) is higher than that at the long gate length(a, L=1 μm)

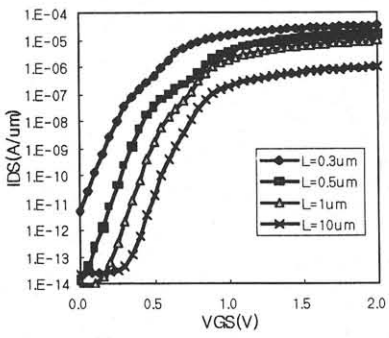


Fig.7(a) The hump simulation results. It clearly shows the dependence of hump on the gate-length. It is strongest at the gate-length of 0.5μm.

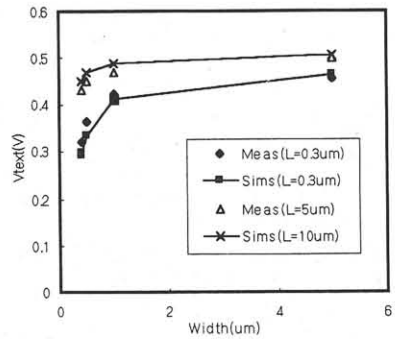


Fig.7(b) The measured and simulated results of the RNWE. The simulated results explain well the RNWE dependence of the gate-length.