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Anomalous Hot Carrier Degradation of nMOSFETs with an Ultra-Shallow Source/Drain Extension

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1. Introduction

As MOSFETs have been scaled down to the sub-quarter micron regime, source/drain junctions (S/D) have been made shallower to suppress short channel effects. In addition, extension structures with higher doping concentrations than the lightly doped drain (LDD) structure have been inevitable to obtain low S/D sheet resistance[1] [2]. These aggressive device designs, aimed at providing high current drivability, have consequently, caused high electric fields around the drain.

We have investigated the effect of shallow junctions on the hot-carrier (HC) reliability of sub-quarter-micron nMOSFETs fabricated by changing process conditions such as the extension implantation dose, the implantation angle, and the punch-through stopper implantation dose. We have found that a shallow junction accelerates LDD-type HC degradation, but that this degradation can be suppressed by increasing the extension-implantation dose or by using an implantation angle over 10°.

2. Device Fabrication

For the n-channel MOSFET fabrication, a conventional LOCOS isolation process was used. Following a growth of a 4- or 5-nm-thick gate oxide layer, the gate electrode was patterned. Then As ions were implanted for the extensions at an ion acceleration energy of 10 keV. Pocket punch-through stopper (PTS) doping was done to suppress the short channel effects. The implantation conditions are shown in Table 1. Following the formation of 100- or 120-nm-thick SiO_2 sidewall spacers, implantation of As was performed for deep S/D formation. Finally, rapid thermal annealing (RTA) at 950 ℃ for 10 s was used to activate the impurities.

3. Results and Discussion

We measured the hot-carrier degradation of the nMOSFETs at various drain-voltage stresses (Vdstress). The gate length of the measured devices was about 0.2 μm. We set the stress gate voltage to the value of maximum substrate current. The drain current in the linear region (Vds = 0.05 V) was measured without exchanging the S/D (the forward bias condition).

Figure 1 shows the change in the linear drain current (I_{dl}) of devices having different pocket PTS doses and different extension doses. The stress drain voltage was 3 V.

The I_{dl} degradation of MOSFETs with a higher pocket PTS dose ($2x10^{13}$ cm^{-2} : devices C and D) was greater than that of MOSFETs with a lower pocket PTS dose ($1x10^{13}$ cm^{-2} : devices A and B). This was because the higher pocket PTS dose caused a higher impact ionization rate (Fig. 2).

For the MOSFETs with the pocket PTS dose of $1x10^{13}$ cm^{-2}, the I_{dl} degradation was almost independent of the extension dose, as devices A and B had almost identical degradation characteristics as shown in Fig. 1. On the other hand, in the MOSFETs with the higher pocket PTS dose of $2x10^{13}$ cm^{-2}, the degradation was greater when the extension dose was $1x10^{14}$ cm^{-2} (device C) than when it was $5x10^{14}$ cm^{-2} (device D). This cannot be attributed to the difference in the impact ionization rate because the impact ionization rate with the $5x10^{14}$ cm^{-2} extension dose was higher than that of the MOSFET with the $1x10^{14}$ cm^{-2} dose.

As previously reported, the lower LDD region dose, the poorer the resistance to HC stress [3] [4]. This well known characteristic of LDD MOSFETs is attributed to an increase in the S/D junction resistance caused by HC trapping beneath the sidewall spacer.

An LDD dose of $1x10^{14}$ cm^{-2} has been considered sufficient to prevent any sheet resistance increase caused by LDD-type HC degradation [5]. This is because the dose is enough to avoid depletion of the extension region even if carriers are trapped beneath the sidewall

Table 1 Process conditions

	device	tox (nm)	sidewall width (nm)	extension dose (cm^{-2})	extension angle (deg.)	pocket dose (cm^{-2})	pocket angle (deg.)
lot1	A	5	100	$1x10^{14}$	0	$1x10^{13}$	0
	B	↑	↑	$5x10^{14}$	↑	↑	↑
	C	↑	↑	$1x10^{14}$	↑	$2x10^{13}$	↑
	D	↑	↑	$5x10^{14}$	↑	↑	↑
lot2	E	4	120	$1x10^{14}$	↑	$2x10^{13}$	↑
	F	↑	↑	↑	10	↑	↑
	G	↑	↑	↑	20	↑	↑
	H	↑	↑	↑	30	↑	↑

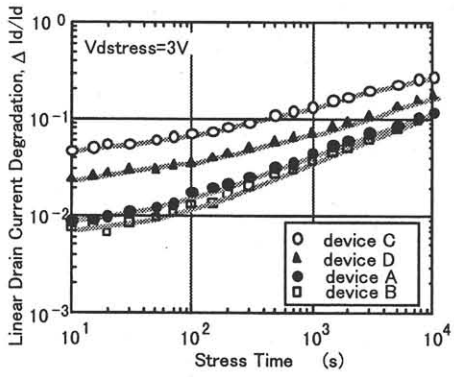

Fig. 1 Degradation of linear drain current. The extension dose and pocket dose were varied as parameters.

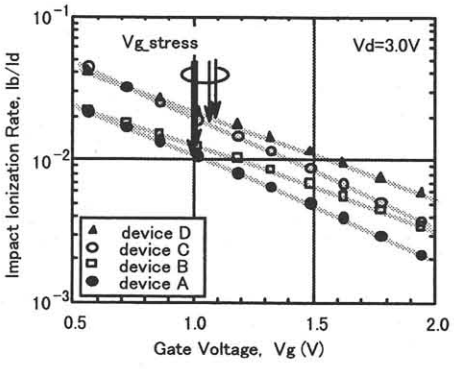

Fig. 2 Impact ionization rate of devices shown in Fig. 1.

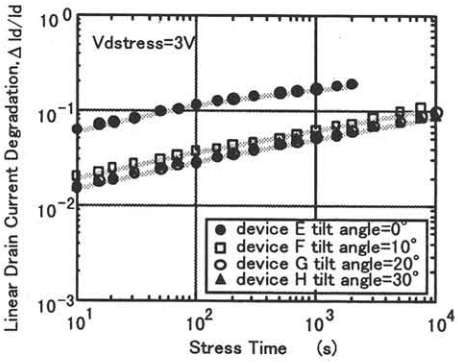

Fig. 3 Degradation of linear drain current. The extension implantation angle was changed as a parameter.

spacers. Also, a relatively large overlap region between the gate electrode and the drain region helps suppress the resistance increase[6]. However, with a decreasing junction depth, MOSFETs become susceptible to HC degradation since the overlap region is also reduced and the maximum electric field approaches the sidewall spacer region.

Figure 3 shows I_{dl} degradation of MOSFETs with extensions made using implantation angles from 0 to 30°. The dose of the pocket PTS and the extension were fixed at $2x10^{13}$ cm^{-2} and $1x10^{14}$ cm^{-2}, respectively. The stress drain voltage was 3 V. The I_{dl} degradation of the MOSFETs with the extension made by vertical

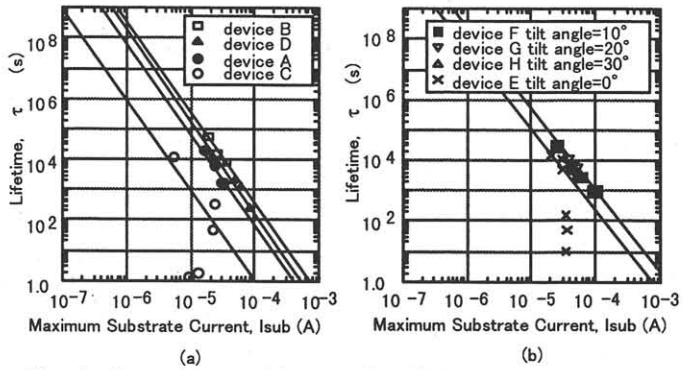

Fig. 4 Dependence of hot carrier lifetime on the maximum substrate current.
(a) the extension dose and pocket dose were varied as parameters.
(b) the extension implantation angle was varied as parameters.

implantation of 0°, which was also used for device C, was the greatest. When the angle was larger than 10°, I_{dl} degradation was drastically reduced, demonstrating the effect of the significant gate-drain overlap.

Figure 4 shows the dependence of the device lifetime on the maximum substrate current. Lifetime was defined as the time at which 10% degradation of the linear drain current in the forward mode occurred. Devices C and E had an anomalously short lifetime. However, the other devices showed normal behavior, and their BVHC (breakdown voltage due to HC degradation defined at 10 years lifetime) was almost 2 V, which satisfies the applied voltage requirement for sub-quarter-micron MOSFETs.

4. Conclusion

Through our investigation of the HC reliability of nMOSFETs with ultra-shallow extensions made by low-energy (10 keV) As ion implantation, we found that that a shallow junction accelerates LDD-type HC degradation due to a reduced gate/drain overlap region. However, this LDD-type HC degradation can be suppressed by using a high extension implantation dose ($> 5x10^{14}$ cm^{-2}) or angled implantation (> 10°).

Acknowledgments

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References

[1]A. Nishida, et al., IEEE Trans. Electron Device, 45, (1998)701
[2]H. Hwang, et al., in *IEDM Tech Dig.*, (1995) 435
[3]F. -C. Hsu et al., IEEE Elec. Device Lett., EDL-5, (1984)71
[4]Y. Sambonsugi, et al., in *Proc. Int. Reliability Physics Symp.*, (1998) 184
[5]M. Kinugawa, et al., in *Symp. VLSI Technol. Dig.*, (1985)116
[6]R. Izawa, et al., IEEE Trans. Electron Devices, 35, (1988)2088