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The Impact of Nitrogen Implantation at LDD(NIL) on Deep Sub-Micron CMOS Devices

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Introduction

Nitrogen contained processes have been well developed for higher reliability and fabrication simplicity. Dual gate oxide can be achieved by nitrogen implantation technique on Si substrate [1]. Oxynitride gate dielectrics are widely used for the suppression of boron penetration in PMOSFET [2]. Nitrogen implantation in source/drain was applied for the hot carrier reliability by reducing the electron trap in sidewall [3]. Additionally, by the suppression of agglomeration of cobalt silicide, nitrogen can give more higher thermal stability [4].

In this work, nitrogen was implanted at LDD region of N/PMOSFETs. Nitrogen atoms interfere with boron and arsenic in channel region. Despite the drastic improvement of hot carrier lifetime by nitrogen implantation at LDD in NMOSFET, NIL technique also develops SCE and degrades I_{ON}/I_{OFF} characteristic as well as lowers effective mobility. On the contrary, nitrogen atoms in PMOSFET results in the improvement of V_{th} roll-off and thus channel length margin. These can be explained by the retardation of boron. Nitrogen directly affects the effective channel length by controlling the boron diffusion in channel direction.

Experiment

Fig. 1 shows the cross-sectional schematic view of CMOS devices. N/PMOSFETs were fabricated by standard 0.18μm gate CMOS technology with 4nm oxynitride gate dielectrics. Nitrogen was implanted in LDD implantation step with the energies of 25~40keV and doses of $9\sim30\times10^{13}cm^2$, as listed in Table I. After the formation of source/drain of MOSFETs, Co-salicide process was performed. The operational voltage(1.8V) are applied to the gate and the drain.

Results and Discussion

As it is well known and shown in Fig. 2, hot carrier lifetime under DAHC injection becomes longer by more than 2 orders in nitrogen implanted NMOSFET. We attribute this improved hot carrier immunity to the improved Si-to-SiO_2 interface state. Fig. 3 shows the plots of lifetime versus impact ionization rate. The slop, *m*, is clearly increased, which is an evidence that nitrogen implantation is effective to the improvement of gate oxide quality.

Fig. 4 illustrates the threshold voltages, V_{th}, are shifted by the nitrogen implantation. This V_{th} decrease is more pronounced for short gate lengths as a result of decreased RSCE in NMOSFET, which is believed due to less boron pileup in the channel region. Unlike NMOSFET, threshold voltages in PMOS devices increase by 120~170mV at L_{gate}=0.18μm, which means the diminution of short channel effect. Threshold voltages are more susceptible to the nitrogen implant dose conditions rather than the energy conditions in both devices.

Nitrogen atoms are known to obstruct the boron's and arsenic's diffusions[3][5]. Moreover, it is believed that the TED of boron is suppressed in channel region. We can estimate the dopant diffusion under the gate edge by measuring the effective channel length. Fig. 5 shows the effective channel length of L_{gate}=0.16μm and 0.2μm, respectively. We observe that the effective channel lengths of NMOSFET become shorter by NIL while L_{eff} of PMOSFET far longer by about 0.025μm with N_2^+, 30keV, $3\times10^{14}cm^2$. Fig. 6 solidifies the control of boron diffusion in the halo of NMOSFET and the p^+ source/drain of PMOSFET. Since the nitrogen occupies the boron diffusion site, the effective boron diffusivity is reduced. In our simulation work, the fitting of V_{th} roll-off is successfully carried out in NMOSFET with a reduced boron pair diffusivity to $7.3\times10^{-8}cm^2/sec$ in the case of N_2^+, 30keV, $3\times10^{14}cm^2$. Therefore, this decline of the effective boron diffusion results in the increase of SCE in NMOSFET and the longer L_{eff} in PMOSFET.

One of the drawbacks of the nitrogen implantation is the degradation of device performance in I_{ON}/I_{OFF} characteristics. Fig. 7 shows I_{ON}/I_{OFF} characteristics of L_{gate}=0.16, 0.18 and 0.2μm, respectively. The I_{ON}/I_{OFF} characteristics are degraded more seriously in NMOSFET. These characteristics result from the decrease of V_{th} as well as the reduction of the effective channel mobility, as illustrated in Fig. 8. The effective channel mobility in NMOSFET tends to fall off by about 5%. However, PMOS devices show no sign of degradation in I_{ON}/I_{OFF} characteristic.

Finally, the nitrogen atoms in LDD region also lead the changes of the gate length margin characteristic. As can be seen in Fig. 9, the length margin is decreased from 17.7nm to 4.6nm in NMOSFET with NIL under the rule of $I_{ON}>500\mu A/\mu m$ and $I_{OFF}<1\times10^{-11}A/\mu m$. However, the length margin is improved by more than 4.3nm under the rule of $I_{ON}>230\mu A/\mu m$ and $I_{OFF}<1\times10^{-10}A/\mu m$ in PMOSFET with N_2^+, 30keV, $3\times10^{14}cm^2$ implantation technique, as illustrated in Fig. 10.

Conclusion

Nitrogen implantation at LDD region has an impact that peculiarly improves HC lifetime by 2 orders in NMOSFET. It is due to the control of the boron lateral diffusion and the robust interface state. We can conclude that the nitrogen implantation technique has some trade-off between the lifetime reliabilities and the device performances such as SCE, the decreased mobility, and the degradation of current drivability in NMOSFET. However NIL can provide more channel length margin in PMOSFET.

References

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[3] S. Shimizu et al., Jpn. J. Appl. Phys., vol. 35, p.802, 1996
[4] W. T. Sun et al., IEEE Trans. ED, vol. 45, p.1912, 1998
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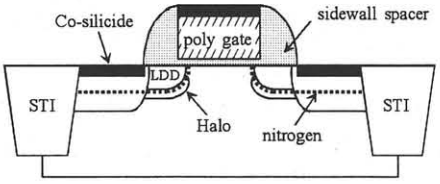


Fig. 1 Schematic view of MOSFET with LDD nitrogen implantation.

Table I. Nitrogen Implantation Conditions

Sample	Energy (keV)	Dose (10^{13} cm^2)
A	25	15
B	30	9
C	30	15
D	30	30
E	40	15

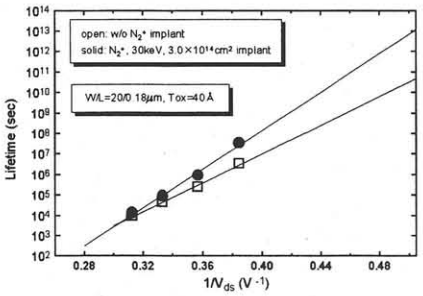


Fig. 2 Dependence of hot carrier lifetime on LDD nitrogen implantation.

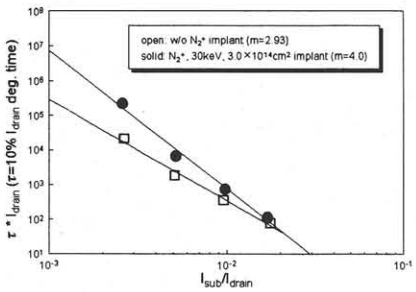


Fig. 3 Comparison of normalized lifetimes with and without nitrogen implantation.

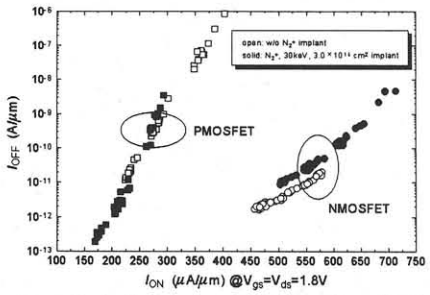


Fig. 7 I_{ON}/I_{OFF} characteristics for MOS devices at V_{ds}=1.8V.

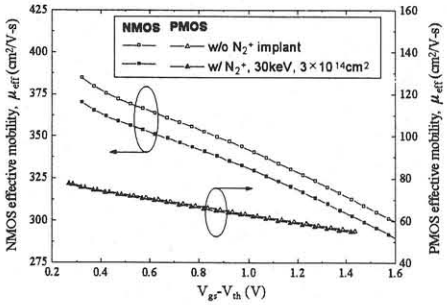


Fig. 8 Degradation of effective mobility in NMOSFET with NIL.

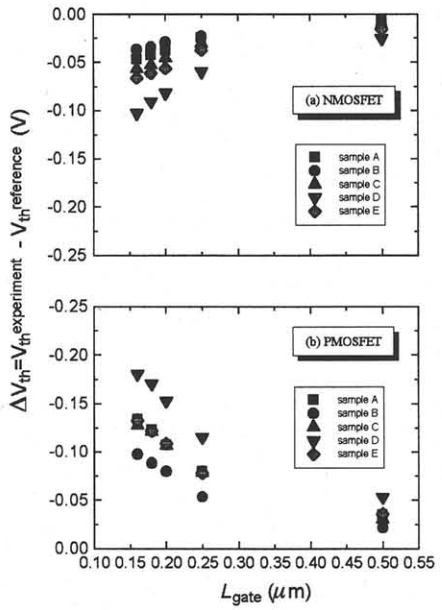
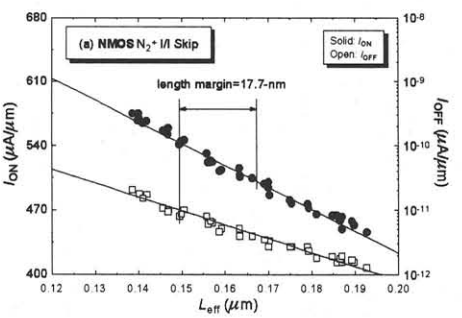


Fig. 4 Plots of threshold voltage, V_{th}, shifts versus the implantation condition.



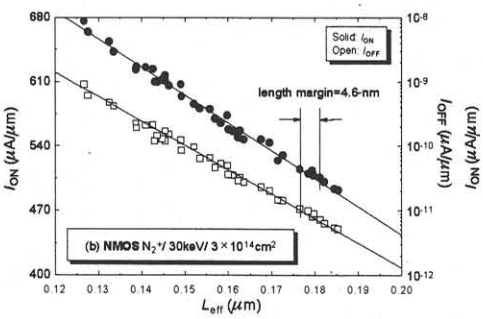


Fig. 9 Degradation of gate length margin characteristics in NMOSFET with nitrogen implantation.

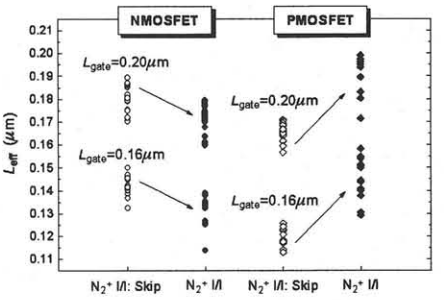


Fig. 5 Reciprocal effects of nitrogen on L_{eff}

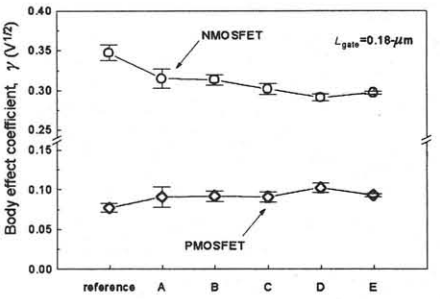
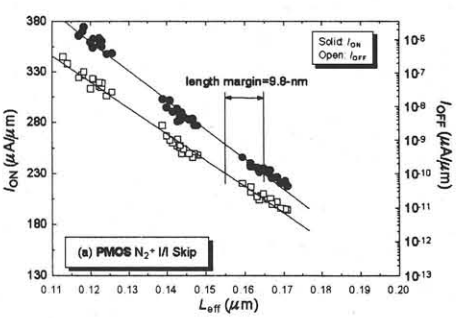


Fig. 6 Dependence of body factor on LDD nitrogen implantation.



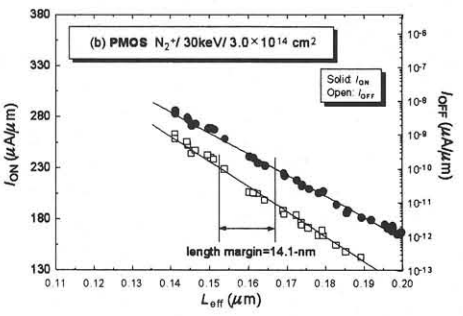


Fig. 10 The improvement of PMOSFET's gate length margin characteristics with NIL.