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Heavy Metal(Cu/Fe/Ni) Behavior in Ultra Thin Bonded SOI Wafers Evaluated by Using Radioactive Isotope Tracers

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1. Introduction

The behavior in silicon for heavy metal elements, which have great influence on device process yield, has been studied for polished wafers and epitaxitial wafers. Since thickness uniformity and crystal quality of SOI (Silicon On Insulator) layer have been improved for thin film SOI wafers, they will be applied to CMOS LSI devices in the near future. However, the behavior of impurity such as heavy metal elements in the thin film SOI has not been investigated because of difficulty of chemical analysis due to thin film silicon layer and due to addition of contamination during evaluation. In this work, the behavior of Cu, Fe and Ni in thin film SOI and BOX (Buried OXide layer) was investigated for the first time by radioactive isotope tracers, which can avoid the evaluation error by contamination from circumstances, and step etching.

2. Experimental Detail

SOI wafer preparation

Specification for sample wafers is shown in Table Ⅰ. Samples were bonded SOI thinned by PACE(Plasma Assisted Chemical Etching). Standard specification was PACE + touch polishing. Wafers with only PACE process were prepared in order to investigate influence of damage introduced by touch polishing. Bonding interface was between BOX and base wafers for standard SOI, but SOI wafers with bonding interface at SOI/BOX (the specification was unfortunately different from other samples) were prepared to examine gettering effects of the interface. Base wafers of SOI were the same specification as reference bulk wafers without intentional gettering site.

Intentional contamination and diffusion annealing

Original RI (Radioactive Isotope) solution and RI adsorptive solution are shown in Table Ⅱ. One side of each wafer (front surface or back side) was immersed in the RI adsorptive solution for 10 min using step-etching apparatus made of PTFE, rinsed for 10 min and dried.

The wafers contaminated with $^{64}Cu/^{57}Ni$ and ^{59}Fe were annealed at 700℃ and 900℃ respectively, in $N_2(2\%O_2)$ ambient for 60min and cooled down at the rate of 3℃/min to 200℃, pulled out of the furnace, and cooled to room temperature. Intentional contamination quantity was $\sim10^{12}$ atoms/cm^2 for each impurity element.

Step-etching and radiation detection

SOI layer, BOX and bulk were etched based on step-etching method reported by Takenaka et. al.[1] to obtain depth profiles of contamination elements. γ -rays of ^{64}Cu ^{59}Fe, ^{57}Ni for etchant and rest part of base wafers after etching were detected by NaI scintillation counter.

3. Results and Discussion

Behavior for Cu

Depth profile of ^{64}Cu is shown in Fig.1. X, Y and Z axes indicate depth direction from wafer surface, sample name, and Cu concentration which 100% is $\sim10^{12}$ atoms/cm^2, respectively. Values in parentheses for X axis show etching removal or the rest part thickness of base wafers with a unit um.

From this result, it was found that Cu could easily diffuse in substrate(or SOI) through BOX layer. Therefore, base wafers with gettering site may prevent SOI active layer from contaminating with Cu in device process. Cu behavior for bulk wafers without BOX layer was almost same profile as SOI wafers. Moreover, as Cu tended to be concentrated at the Si side of bonding interface which was a gettering site for Cu, it is suggested that bonding environment plays a role of Cu gettering at bonding interface. Touch polishing damage didn't have influence on Cu diffusion in SOI wafers.

Behavior for Fe and Ni

Fe and Ni couldn't diffuse in substrate(or SOI) through a BOX layer, while Cu could diffuse in that. But behavior of Fe to oxide layer (BOX and surface oxide) was quite different from Ni. Fe tended to be concentrated in surface oxide and BOX side of BOX/substrate interface. Ni was captured under the surface oxide and in SOI side of SOI/BOX interface. As it is very critical problem for device process that Ni, which is same diffusivity in Si as Cu, can't diffuse to substrate through BOX layer, it is necessary to design useful gettering site in SOI layer or substrate for Ni.

4. Summary

Cu was able to be diffused through BOX layer easily, and bonding interface was a gettering site for Cu.

Fe tended to be concentrated in BOX side of BOX/substrate interface, and was not diffused through BOX layer.

Ni tended to be concentrated under the SOI surface oxide and in SOI side of SOI/BOX interface, and was not diffused through BOX layer.

Results of defect evaluation for rest part of substrates after etching will also be reported in the presentation.

5. Acknowledgments

The authors would like to thank Nagano-Denshi Co., Ltd. for supplying PACE'd SOI wafers. Intentional contamination by radioactive isotope, diffusion annealing, step-etching and RI tracer analysis were supported by Purex Co., Ltd, which is gratefully acknowledged.

6. Reference

[1] M. Takenaka, M. Tomita, A. Kubota, N. Tsuchiya and H. Matsunaga: BUNSEKI, 173, (1994)

Table I. Specification of sample wafers(150mmΦ,<100>)

Samples	SOI layer			BOX	Base wafers
	thickness	Res.	P/N	thickness	(crystal/type/Res./thickness)
PACE + Touch Polishing(T.P.)	0.5um	10-15Ωcm	P	0.5um	CZ/P/ 15Ωcm/625um
PACE only	0.5um	10-15Ωcm	P	0.5um	CZ/P/ 15Ωcm/625um
Reverse bonding interface (SOI/BOX is bonding interface)	0.5um	0.006Ωcm (Sb diffusion)	N	1.2um	CZ/P/ 0.08Ωcm/625um
Polished wafers(Ref.)	CZ/P/~15Ωcm/625um				

Table II. RI solution preparation

RI / Solution	^{64}Cu	^{59}Fe	^{57}Ni
Original RI solution	Cyclotron→ Chemical separation→ HNO_3 solution	$^{59}FeCl_3$→ Dilution by HCl solution	Cyclotron→ Chemical separation→ HNO_3 solution
Adsorptive solution	Original RI+BHF	Original RI+SC-1	Original RI+SC-1

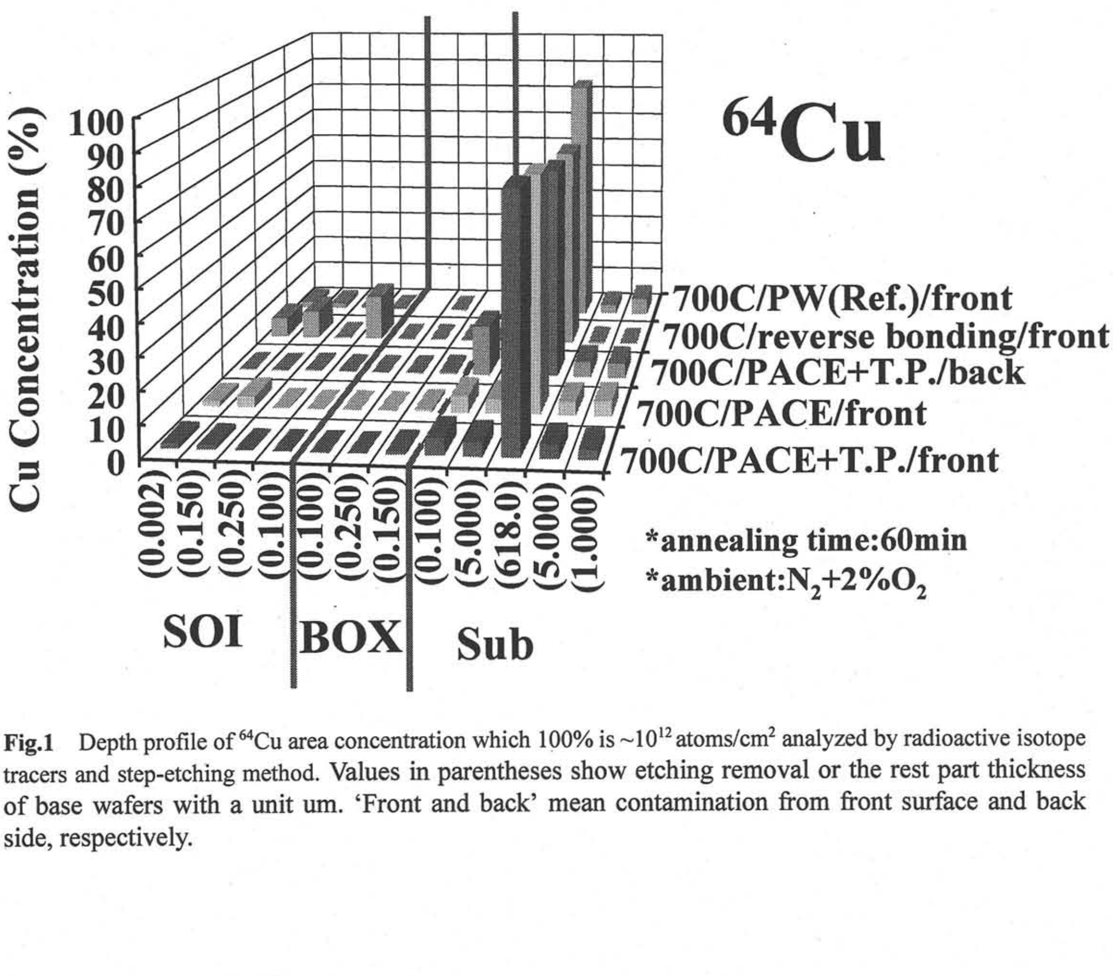

Fig.1 Depth profile of ^{64}Cu area concentration which 100% is ~10^{12} atoms/cm^2 analyzed by radioactive isotope tracers and step-etching method. Values in parentheses show etching removal or the rest part thickness of base wafers with a unit um. 'Front and back' mean contamination from front surface and back side, respectively.