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AC Floating Body Effects and 1/f Noise Characteristics of Dual Body SOI Structure for Analog-Digital Mixed Mode Circuit

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ABSTRACT — New SOI structure for mixed analog-digital applications is proposed where analog and digital MOSFET's are independently optimized. Two types of field oxide are introduced so that the body bias of analog devices can be effectively controlled whereas the channel region for digital devices is fully depleted. From measurements and modeling of the body related device characteristics such as the AC and 1/f noise, it is shown that the proposed structure can be a strong candidate to the future the SOI technology for mixed analog-digital circuit applications.

1. INTRODUCTION

In the thin film SOI CMOS technology for mixed analog-digital circuit applications, it is difficult to suppress the degradation in the source/drain resistance and the unwanted SOI floating body effects such as the kink, low voltage breakdown, and noise. Various body-tied structures have been proposed to overcome the kink effect adopting a thick silicon film [1], [2]. However, the structure may not be optimal for the digital application. In this paper, we introduce a new structure having the body-tied SOI device for analog application and fully depleted SOI device for digital application with thick source/drain built on the same wafer. Two types of field oxide make possible to control independently the body bias of each device. Device characteristics such as AC body instability, and the flicker noise level are investigated for both analog and digital MOSFET's on the same wafer. Advantage of the new technology to independently optimize the analog-digital devices is shown.

2. DEVICE FABRICATION

A schematic cross sectional view of the processed structure is shown in Fig. 1. This structure consists of two regions; the digital circuit region where the channel region of MOSFET is recessed (***digital MOSFET***) [3] so that source/drain regions are formed on a thick film, and the thick film part for the analog circuit region (***analog MOSFET***), where the channel is partially depleted and the body has a contact. An n-field threshold control implantation with the energy of 90 keV-Boron and dose of 4E12, 8E12, and 5E13 cm^{-2} has been performed so that Rp (ion implant peak) is located under the mini-field whereas Rp is located below the device channel region [4].

3. DEVICE CHARACTERISTICS

The fully depleted digital MOSFET has the similar source/drain resistance value as the analog devices since it has thick source/drain regions, and this advantage will become more apparent if the salicide process is employed.

Dynamic floating body effect in PD SOI device is a serious problem especially in the analog circuit so that it is currently under a serious research topic. It is important to accurately estimate body resistance and the body voltage as a function of gate pulse frequency. We extract the body voltage (V1) in Fig. 2(a) through the measured body contact voltage (V2) and the simple model. Fig. 2(a), (b), and (c) show the cross sectional view of the transistor (W/L = 100/100) in the width direction, the equivalent circuit and equations for V1 and V2 written as function the V_{GS}, respectively. Fig. 3(a) shows a comparison between the measurement and the simulated body contact voltage when gate pulses with rise time and falling time of 30 ns are applied. R_{body} values taken from the measurement are used for the simulation. Fig. 3(b) shows that the extracted V1 voltage increases as the body resistance increases for a fixed frequency. Now we measure the DC I_D change due to the change in the body voltage (V1) in Fig. 3(c). If the rising/falling time in the output of pulse generator is zero, no difference exists between DC I_D and AC I_D. But the existence of a finite rising/falling time makes AC I_D decrease as frequency increases, as denoted by the dotted line. However, actual measurement shows that I_D increases with the increase of the frequency, which is due to the body voltage increase. The data denoted by circle symbols are the net increase in the I_D due to the floating body effect.

On the same wafer, the flicker noise is measured for the analog and the digital MOSFET's, which is important in mixed mode analog-digital circuits. The flicker noise characteristics of conventional FD and PD SOI device, independently, have been reported [5]. For the first time, we report the 1/f noise of the recessed channel FD (digital MOS) and PD MOSFET's (analog MOS) on the same wafer. Fig.4 shows the flicker noise characteristics for the digital and the analog MOSFET's with short channel at I_D = 35.61 μA (a), long channel at I_D = 35.61 μA (b), and long channel at I_D = 11.87 μA (c). In general, noise source effects due to traps and G-R center in short channel devices are larger than long channel one. Thus the noise power spectral density of short channel device is larger than that of long channel device for the same I_D. The analog MOSFET's show much lower flicker noise level, because the neutral body present in the analog MOSFET prevents the effect of the back-interface trapping and detrapping from interacting with the front channel.

4. CONCLUSIONS

We proposed a new SOI structure for analog-digital mixed mode applications. Various device characteristics such as the short channel effect, S/D resistance, and the body resistance related characteristics (transient body instability), and 1/f noise characteristics have been demonstrated. It is shown the proposed structure has a potential for the optimization of the analog and digital devices.

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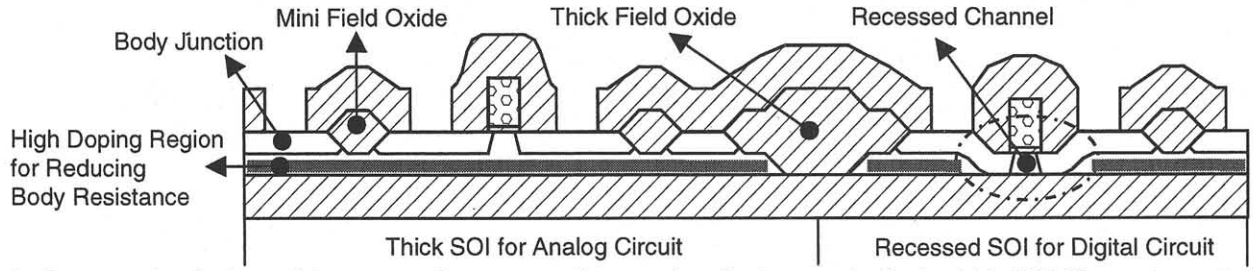
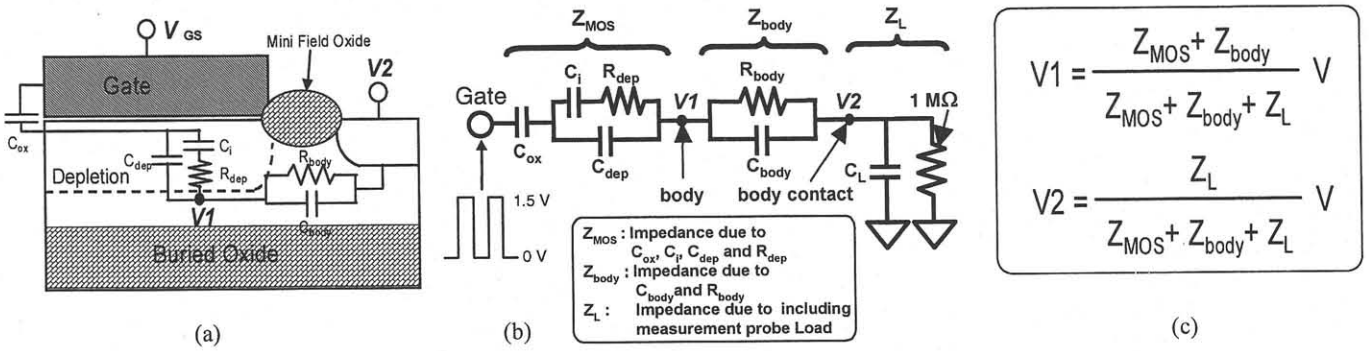
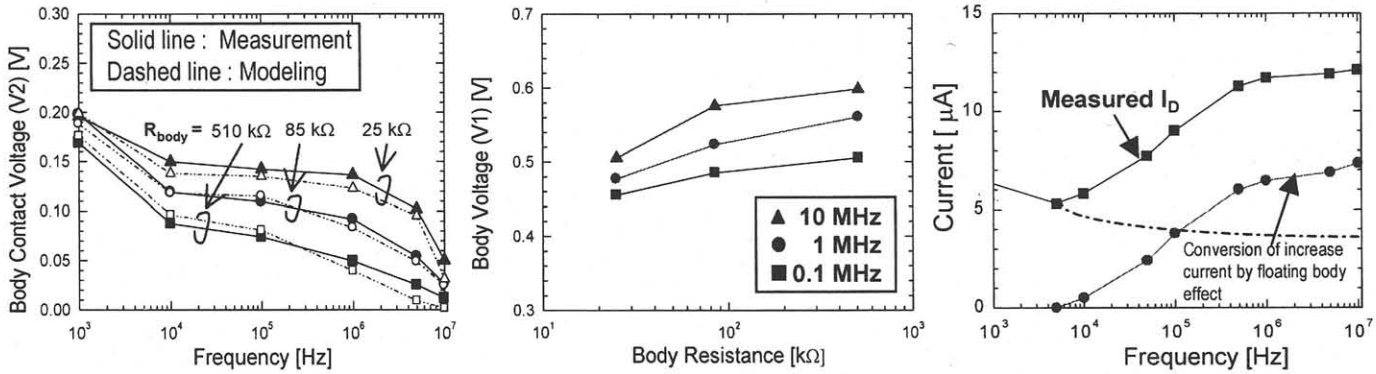


Fig. 1. Cross sectional view of the proposed structure where analog devices are built in thick SOI film region and digital devices are built in recessed channel region.



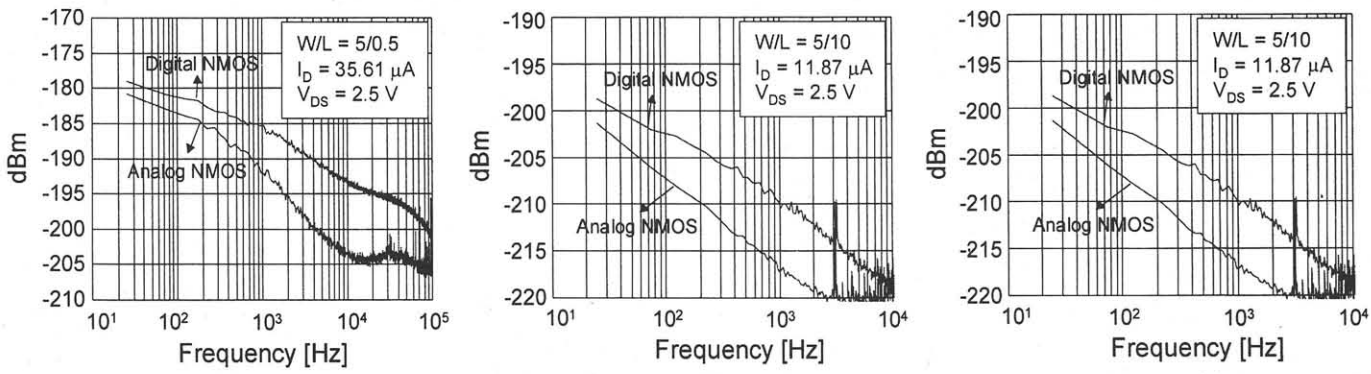
(a) (b) (c)

Fig. 2. (a) Cross-sectional view of MOSFET in the width direction. (W/L =100/100 μm). Non-uniformity in the S/D direction is ignored. (b) equivalent circuit of (a), and (c) equations for extraction of V1 and V2.



(a) (b) (c)

Fig. 3. Transient body instability characteristics. (a) measurement and modeling value of V2 vs. gate frequency. (b) modeling value of V1 vs. body resistance. (c) Measured drain current vs. gate frequency.



(a) (b) (c)

Fig.4. Drain current 1/f noise power spectral density characteristics for the digital and the analog NMOSFET's. (a) I_D = 35.61 μA and V_{DS} = 2.5 V (W = 5 μm, L_{eff} = 0.5 μm), (b) I_D = 35.61 μA and V_{DS} = 2.5 V (W = 5 μm, L_{eff} = 10 μm), (c) I_D = 11.87 μA and V_{DS} = 2.5 V (W = 5 μm, L_{eff} = 10 μm).