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Inherent Suppression of Low-Frequency Noise Overshoot in Sub-Micron Partially-Depleted Floating Body Silicon-On-Sapphire (SOS) MOSFETs

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1. Introduction

CMOS built on silicon-on-sapphire (SOS) is attractive not only because sapphire (Al_2O_3) provides a lossless substrate with 2x the thermal conductivity of silicon [1], but it also exhibits inherent weaker kink effect in partially-depleted (PD) operation mode than PD SOI/SIMOX technology, as shown in Fig. 1. The latter is due to a much larger junction leakage resulting from the mismatch between silicon and sapphire atoms in the silicon/sapphire interface [1]. One remaining issue for the implementation of SOI CMOS technology in RF applications is low-frequency noise [2], which can be divided into two aspects: one is oxide quality related GR noise and the other is floating body induced Lorentzian-like noise overshoot. In this study, we show that a higher source/body junction leakage current in an advanced SOS technology results in an inherent suppression of Lorentzian-like noise overshoot without the degradation of flicker noise.

2. Devices and Measurements

Peregrine Semiconductor's UTSi® technology, using the single solid phase expitaxy (SSPE) regrowth technique, provides a low defect density silicon film with a final thickness of 100nm and electron and hole mobility similar to those found in bulk silicon [3]. Surface channel PD floating body submicron SOS MOSFETs were used in this study with 12nm gate oxide thickness. On-wafer low-frequency (LF) noise measurement were conducted using an HP 3561A dynamic analyzer, an EG&G 5113 low noise amplifier, a probe station, and a DC bias network.

First of all, the PD SOS nMOSFET was biased in the pre-DC kink region to examine LF noise characteristics. With reduced stress during silicon regrowth on sapphire by reducing amorphization temperature, excess GR noise has been suppressed and a pure $1/f$ noise is achieved in an advanced SOS technology (Fig. 2). Fig. 3 further shows that the latter demonstrates the pure $1/f$ noise spectra in a wide V_{GT} ($V_{GS} - V_{TH}$) range without the existence of GR noise in the subthreshold region. In addition, the input-referred gate noise is independent of V_{GT}. These results indicate that the flicker noise in advanced SOS MOSFETs is governed by the McWhorter number fluctuation model [4], due to the trapping/detrapping of conducting carriers by the front gate oxide traps, and there is no bulk trap-related GR noise.

Fig. 4 shows the impact of the floating body effects on the LF noise of a 0.65μm PD floating body SOS nMOSFET. It shows that there are Lorentzian-like noise spectra occurring with corner frequency (f_0) higher than 6kHz superimposed on the existing $1/f$ noise with V_{DS} above 1.5V. In addition, f_0 shifts towards higher frequency and the peak magnitude of relative noise overshoot (@ f_0) increases as V_{DS} increases. More importantly, this phenomenon is different from the LF noise overshoot in PD floating body SOI/SIMOX nMOS where f_0 shifts from below 1Hz to above MHz as V_{DS} increases from the DC kink onset [5]. Rather, it is similar to those found in FD SOI/SIMOX devices [6].

3. Discussion

Low-frequency Lorentzian-like noise overshoot characteristics in PD SOI/SIMOX nMOS have been correlated with AC kink effect [5], suggesting that the overshoot noise are caused by the body current fluctuation amplified by the frequency dependence of the source/body (S/B) junction impedance [7]. More importantly, the influence of the S/B junction characteristics need to be taken into account to develop a comprehensive excess noise model as follows [8],

$$S_{VG,excess} = 2q(nV_T)^2 \frac{1}{1+(f/f_0)^2} \cdot \frac{I_{SB}}{(I_R + I_{SB})^2} \cdot \beta^2 \quad (1)$$

where $\beta = \partial V_{TH}/\partial V_{BS}$ and I_R is the S/B junction diode saturation current. Thus, the suppression of noise overshoot in PD SOS nMOS suggests that its AC kink effect is similar to those in FD SOI/SIMOX devices. This is evidenced by the convergence of AC G_{DS} curves up to 10kHz (Fig. 5). In SOS technology, the traps existing in the buried silicon/sapphire interface drastically increase I_R. As devices are biased above the DC kink, the body is mainly charged by the impact ionization current (I_{ii}). In the V_{DS} region where $I_{SB} \approx I_{ii} \ll I_R$, the LF noise overshoot in SOS nMOS device diminishes (as expected in (1)) until V_{DS} is large enough that $I_{ii} \gg I_R$. As a result, a higher I_R in SOS technology inherently suppresses the LF noise overshoot phenomenon at the operation region where I_R overwhelms I_{ii}, leading to the occurrence of noise overshoot only at higher frequencies. The excess noise in the lower frequency range (< 10kHz) is suppressed, as is the AC kink. Scaling down the channel length reduces the S/B junction potential barrier (due to a larger DIBL), resulting in a larger I_R. Figure 6 shows the LF noise characteristics of a 0.35μm SOS nMOS device. Compared with those in a 0.65μm device (Fig. 2), the increase of I_R further suppresses the Lorentzian-like noise overshoot resulting in a higher f_0 and a smaller noise overshoot amplitude. Consequently, deep submicron PD floating body SOS CMOS technology enables the designer to implement low power RF circuits without using the extra body contacts or shifting towards more fully-depleted operation.

4. Conclusion

In this study, the low-frequency noise characteristics in thin film PD floating body SOS nMOS have been examined.

The results indicate that the higher I_R in SOS CMOS technology results in the suppression of Lorentzian-like noise overshoot. In addition, the achievement of comparable flicker noise level with SOI/SIMOX and silicon bulk nMOS technology [9] suggests that there is no obvious degradation on LF noise due to back silicon/sapphire interface coupling. Therefore, inherent weaker floating body effects in SOS CMOS technology implies that it can be a potential candidate for the integration of a communication system on a single chip.

References

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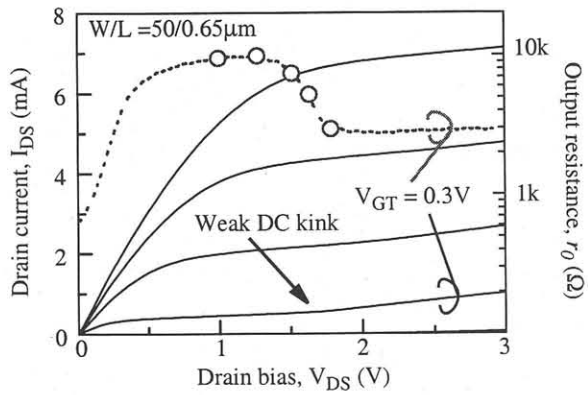

Fig. 1 Output characteristics of a PD floating body SOS nMOS as a function of V_{GS}: from 0.5V to 2.5V with 0.5V step. The dashed line shows the output resistance measured at V_{GS} = 1V (V_{GT} = 0.3V) and the circles indicate the DC bias points for noise measurement.

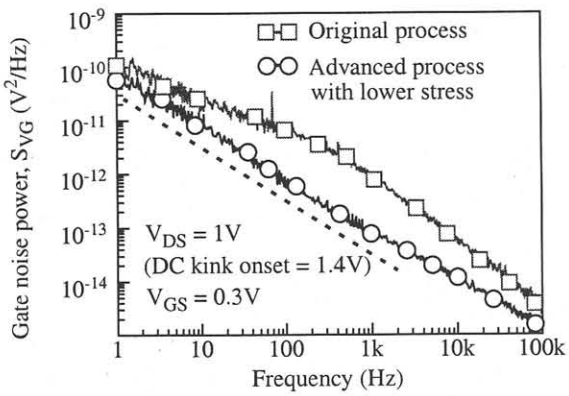

Fig. 2 Low-frequency noise characteristics of 0.65μm PD floating body SOS nMOS, showing the improvement by reducing amorphization temperature. Dashed line represents ideal $1/f$ noise.

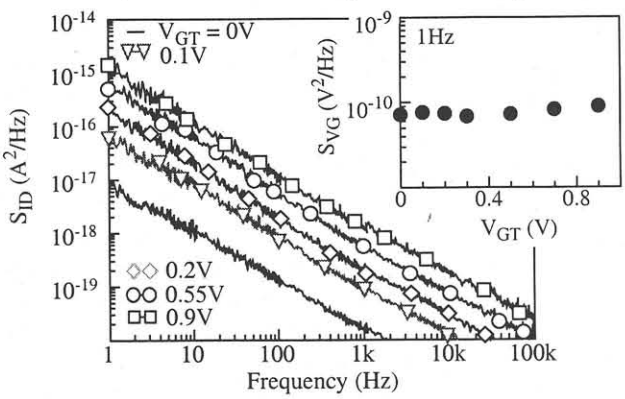

Fig. 3 Output current noise power of a PD floating body SOS nMOS as a function of V_{GT} biased at V_{DS} = 1V with W/L = 50/0.65μm. The inset shows the spot noise measured at 1Hz (S_{VG} @1Hz) versus V_{GT} in saturation region.

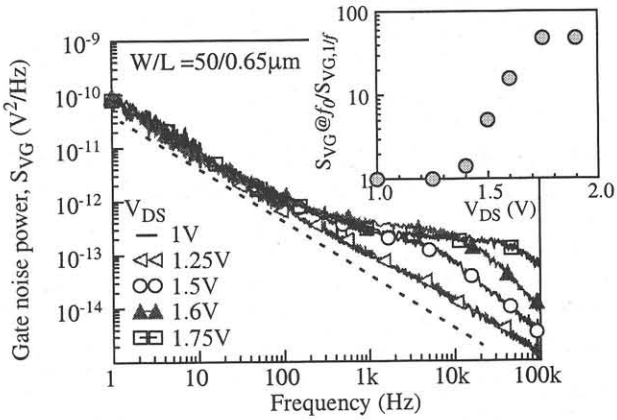

Fig. 4 Equivalent input-referred gate noise power spectrum versus frequency of a PD floating body SOS nMOSFET as a function of drain voltages biased at V_{GT} = 0.3V. The inset shows the peak magnitude of relative noise overshoot.

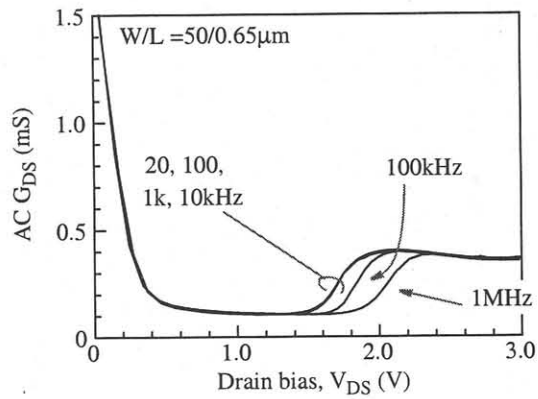

Fig. 5 AC output conductance of 0.65μm PD floating body SOS nMOS as a function of measured frequencies, biased at V_{GT} = 0.3V.

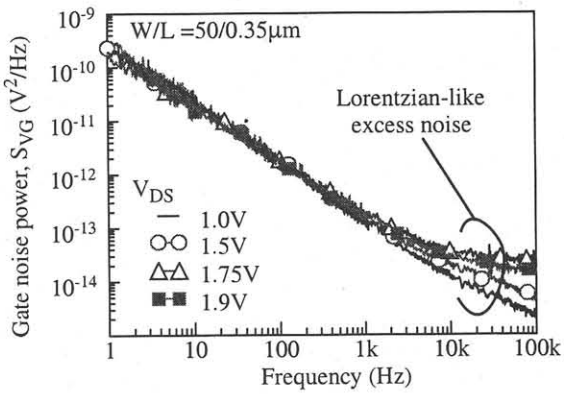

Fig. 6 Equivalent input-referred gate noise power spectra versus frequency of a 0.35μm PD floating body SOS nMOS as a function of drain voltages biased at V_{GT} = 0.3V.