Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 496-497

Invited

Copper Metallization for High-Speed ECL-CMOS LSI's

N.Ohashi, T.Saito, T.Hashimoto, J.Noguchi, T.Imai, K.Sasajima,
H.Yamaguchi, and N.Owada

Device Development Center, Hitachi, Ltd.,
16-3, Shinmachi 6-chome, Ome, Tokyo 198-8512, Japan
Phone:+81-428-33-1111 Fax:+81-428-33-2164

Abstract

Cu metallization technology using sputtered Cu wiring is developed. Submicron trenches for wiring with even 0.4μm in width are filled with Cu by a low-pressure long-throw sputtering method followed by a reflow process. Using these technologies, multilevel Cu metallization test structures are fabricated successfully. Cu metallization technology reduced wiring delay time on a test chip by about 30%.

Introduction

A Cu damascene process is one of the most important technologies to realize the Cu metallization structures for high-speed logic LSI's. Recently, various Cu deposition methods such as CVD, electroplated are studied to fill trenches and holes for wiring (1)(2)(3). Among these deposition methods, sputtering technology has very large amount of technology bases and this technology is well understood and widely used in the LSI industry. So, we applied the newly developed sputtering technology combined with reflow process to Cu filling process (4)(5), resulting in successful formation of the multilevel metallization test structure.

Experimental

For wiring formation, sequential sputtering deposition of TiN and Cu films on patterned wafers was performed. Cu films were deposited by the sputtering method with the operation pressure varied from 1.8E-2Pa to 3.0E-1Pa and target to substrate distance varied from 170mm to 140mm without wafer heating. After sputtering deposition, wafers were annealed to flow the Cu films and to fill the submicron trenches and holes at 450℃ for 5min.. After reflow process, Extra Cu and TiN were removed using CMP, and Cu wiring structure was formed. Using this process, multilevel Cu metarrization test structure was fabricated, and electrical characteristics were evaluated.

Results and Discussion

Fig.1 shows the minimum bottom coverage of as-deposited Cu films on trenches and holes as a function of target to substrate distance, suggesting that longer target to substrate distance improves the bottom coverage. Fig.2 shows the effect of reduced operation pressure for improved bottom coverage. At the range of operation pressure below 1E-1Pa, bottom coverage is improved because the scattering of sputtered Cu atoms caused by Ar atoms decreases. Approximately 70% bottom coverage is achieved for the trench whose aspect ratio is 1.6 with the target to substrate distance of 300mm and in the operation pressure of 1.8E-2Pa without additional heat treatment. Under this condition, the deposition rate of Cu is over 350nm/min. with the target DC power of 12kW.

Higher aspect ratio reduces the as-deposited bottom coverage especially in case of holes rather than trenches because the angular divergence of sputtered Cu atoms which can reach the inside of trenches and holes becomes narrower. So a reflow process was also studied to fill not only long trenches but also short trenches and holes. Fig.3 shows the bottom coverage of Cu films before and after 5min. annealing as a function of trench length. As the trench length becomes shorter, bottom coverage before annealing becomes poorer. On the other hand, as clearly indicated in this figure, the 5min. annealing improves the bottom coverage of Cu films resulting in successful filling of trenches and holes.

After the reflow process, extra Cu and TiN were removed using CMP process to form Cu wiring, and wiring delay was measured by using ECL ring oscillataors. This result is shown in Fig.4, Cu metallization reduced wiring delay time on a test chip by about 30%. Thickness of Cu wiring of signal lines was reduced to half that of Al wiring. Small parasitic capacitance of interconnects is expected to have acheived the reduction in clock wiring delay.

Using these technologies, multilevel Cu metallization test

structures are fabricated successfully. Fig.4 shows the cross sectional SEM of 7 level metallization test structure. Cu metallization was used for the signal lines of metal-2 to metal-5 levels. Thin Cu layer were used in metal-2 and metal-3 in order to suppress interconnect capacitance in fine-pitch signal lines. In these layer, the narrowest wiring is 0.4μm in width and 1.2 in aspect ratio. And thick Cu layers were used for metal-4 and metal-5 in order to reduce interconnect resistance in long lines. As is clearly shown in this figure, the narrow Cu wiring in this structure is nicely filled with our developed sputtering technology.

Conclusion

Submicron Cu wiring is formed by the low-pressure and long-throw sputtering technology combined with the reflow process. Lower operation pressure and longer target to substrate distance improve the bottom coverage of Cu film. Cu metallization suppresses parasitic capacitance of interconnects and reduces clock wiring delay by about 30%.

Using these technologies, it is demonstrated that the submicron Cu multilevel metallization test structure with 0.4μm width Cu wiring are successfully formed.

Reference

1) F.B.Kaufman, et al., J.Electrochem. Soc. (1991) 138, 3460.

2) M.Hoshino, et al., in Advanced Metallizaiton and Interconnect Systems for ULSI Application in 1995, (Mater. Res. Soc. Proc., Pittsburgh, PA, 1996) pp.701-707.

3) V.M.Dubin, et al., in Proceedings of 1997 International VLSI Multilevel Interconnection Conference, pp.69-74.

4) T.Saito, et al., in Advanced Metallizaiton and Interconnect Systems for ULSI Application in 1996, (Mater. Res. Soc. Proc., Pittsburgh, PA, 1997) pp.149-154.

5) T.Saito, et al., in Proceedings of 1998 International Interconnect Technology Conference, pp.160-162.

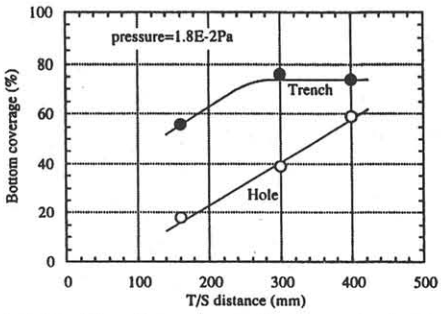

Fig.1 The minimum bottom coverage of Cu films as a function of target to substrate distance.

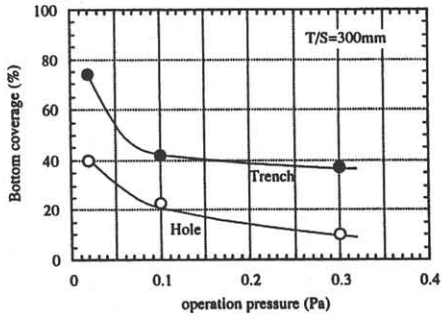

Fig.2 The minimum bottom coverage of Cu films as a function of operation pressure.

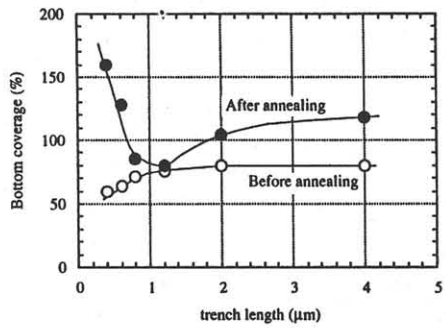

Fig.3 The minimum bottom coverage of Cu films as a function of trench length.

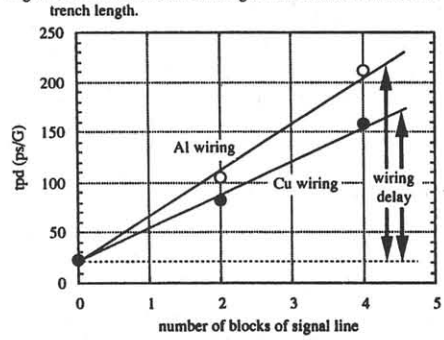

Fig.4 Dependence of propagation delay time on wiring length.

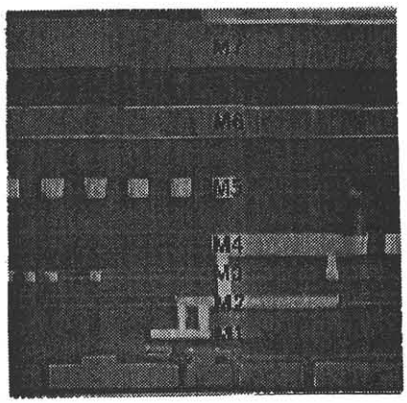

Fig.5 Cross sectional SEM photograph of 7-level metallization test structure.