Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 498-499

A Reliable Interconnection Technology Using Organic Low-K Dielectrics for 0.18 μm CMOS Circuit

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1. Introduction

As the dimensions of ULSI devices continue to shrink, the RC delay of interconnects will limit the device speed performance. A major component of the delay arises from the capacitance of Inter Metal Dielectric (IMD). In order to decrease the capacitance, organic polymers [1], organic spin-on glass (SOG) [2], and inorganic SOG (hydrogen silsesquioxane; HSQ) [3] have been proposed. However their thermal stability, adhesion and mechanical strength need further improvement to be used in the ULSI fabrication process [4].

In this paper, we succeeded to introduce poly-arylethers (PAE:K=2.8) film into the W-plug/Al wiring interconnection. Its effects were demonstrated by the delay time of CMOS circuit and via contact yield.

2. Process Sequence

The schematic cross section of our test device is shown in Fig. 1. After 1st Al-Cu metal wiring was pattered, PAE source was spun-on coated and cured. PECVD silicon dioxide is deposited above the organic low-K film. SiO2 film also acts as a etching mask of PAE. The PAE/SiO2 film was planarized by CMP. The PAE was etched by electron cyclotron resonance (ECR) etching system using N2/He gas mixture [5]. W-plug filling is performed by Blanket CVD-W deposition and etch back process. After via-plug formation, upper 2nd Al-Cu metal was fabricated. This process sequence would be repeated to proceed multilayer fabrication.

Fig. 2 shows a SEM cross section for a W via plug/Al wiring interconnect structure (Via hole=0.24 μ m$^{\phi}$, 0.9 μ m depth). In this photograph, the thickness of PAE/SiO2 at via hole are in ratio 1 : 2.5. Via holes were completely filled by CVD-W without any voids. And the PAE has good adhesion between the Al-Cu metal layer and PECVD silicon oxide layer.

3. CMOS Integration

First, we verified the dielectric constant in wire-to-wire space with PAE. Experimental data was compared with results of intra-level capacitance simulation. As shown in Fig. 3, measured results give a good agreement with calculation. The intra-level dielectric constant was uniformly reduced from 4.2 to 2.8 .

In order to demonstrate the impact of reduction in intra-level capacitance, we measured the electrical characteristic on 0.18 μ m CMOS circuit. The reference sample was fabricated with conventional silicon dioxide dielectrics. Fig. 4 shows there was no difference in gate delay time of simple F/O=1 inverter. Low-K process does not affect any influence on the device characteristics. However, the effect of low-K dielectric is measured by ring oscillator delay time with wiring load. As shown in Fig. 5, stage delay time of inverter was improved in our low-K process. In comparison with the conventional silicon dioxide interconnect, stage delay time of inverter with 1mm wiring load length was reduced by 16%. Fig. 6 shows the measured ring oscillator delay of NAND circuit as functions of the wiring load length. The stage delay time increased in comparison with inverter. This difference is explained by number of gate and contact electrode.

Finally, in order to apply the low-K technology to an advanced 0.18 μ m CMOS process, influence of the PAE on via resistance was evaluated. The measured via resistance for 0.24/0.26/0.28/0.30 μ m vias in the Al/W-plugs/low-K interconnects are shown in Fig. 7 for Kelvin single via structure. The average resistance at 0.24 μ m$^{\phi}$ was 7.5 Ω and good uniformity was obtained in a whole wafer. Fig. 8 shows the measured resistance for 144K via chains of via size 0.24/0.26/0.28/0.30 μ m. A 100% yield was obtained for the all via sizes. There is no difference between the low-K process and conventional silicon dioxide process. These results indicate that a reliable Al/low-k interconnect has been achieved.

4. Summary

We developed W-plug/Al wiring interconnection process using PAE. Low via contact resistance and 100% yield were obtained. This process was promised to apply the advanced logic LSIs.

Acknowledgments

The authors would like to thank Mr. Shinichi Hishikawa for his continuous encouragement.

References

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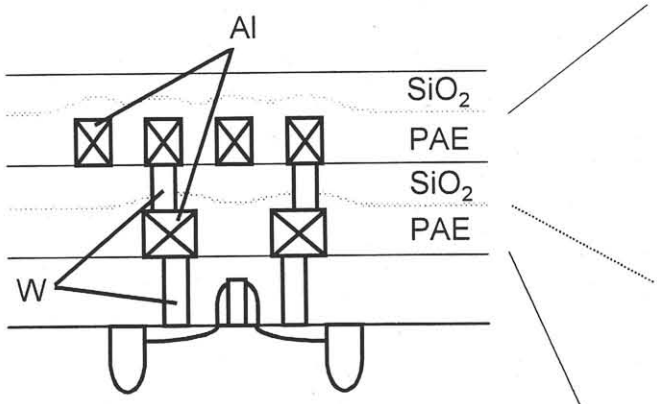


Fig. 1 Schematic diagram of test device structure.

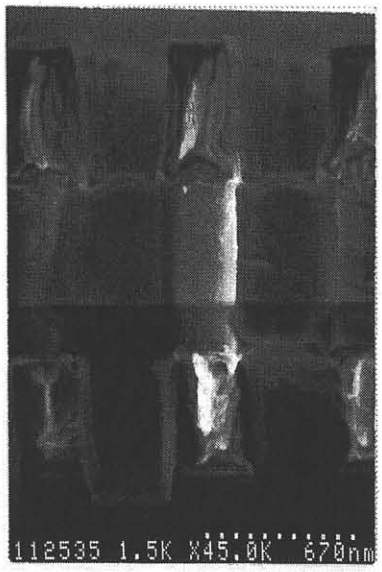
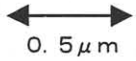


Fig. 2 SEM photograph of the cross-sectional view of double layered interconnection.



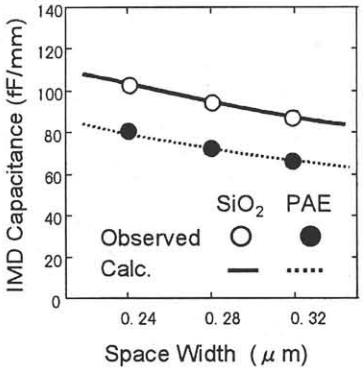


Fig. 3 IMD capacitance vs. space width.

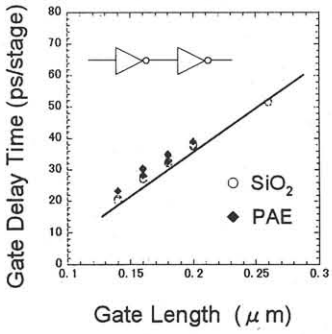


Fig. 4 Gate delay time vs. gate length. Tox=3.5nm. Wn/Wp=1.8/3.6 μm. Vdd=1.8V.

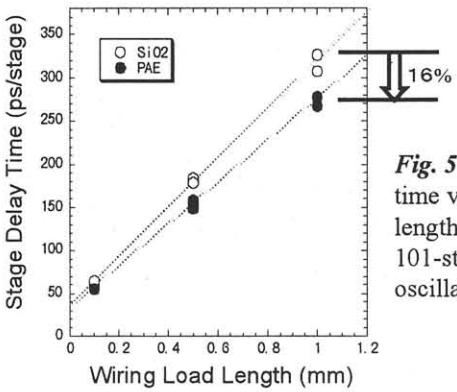


Fig. 5 Stage delay time vs. wiring load length on the Inverter 101-stage ring oscillator (FO=1).

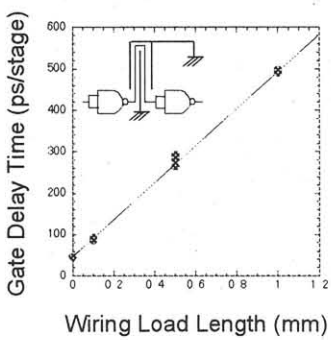


Fig. 6 Stage delay time vs. wiring load length on NAND 101-stage ring oscillator. Wn/Wp=1.8/1.8 μm FO=1. Vdd=1.8V

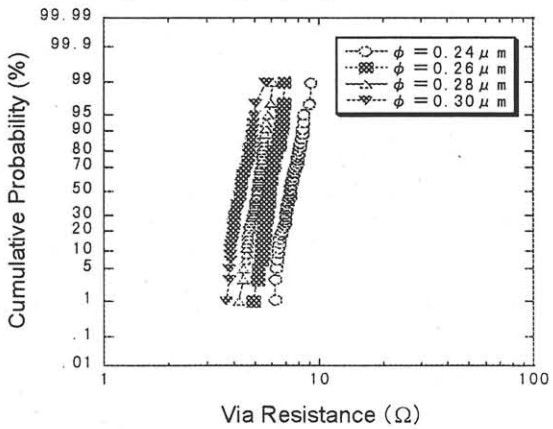


Fig. 7 Via resistance measured by Kelvin contact pattern.

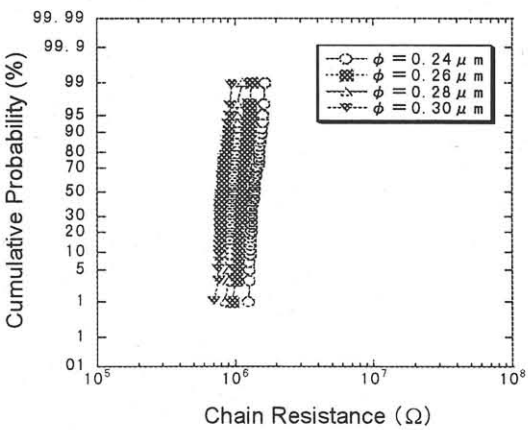


Fig. 8 144k via chain resistance.