A Novel and Low Thermal Budget Planarization Scheme for Pre-Metal Dielectric Using Electron-Beam Cured HSQ (Hydrogen Silsesquioxane) in STC (Stacked Capacitor) DRAM

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Abstract

We investigated a new planarization process by employing an E-beam (electron-beam) cured HSQ (hydrogen silsesquioxane) based inorganic SOG (spin-on-glass) for pre-metal dielectric materials, in order to develop a simple planarization process with low thermal budget and good planarity in STC (stacked capacitor) DRAM devices, and achieved lower leakage current and higher capacitance for Ta2O5 capacitor as well as better planarization performance than those of conventional USG etch back process. No degradation of device characteristics such as Vth change or hot carrier hardness, and gate oxide quality has been observed.

Introduction

Densification of DRAM requires increase of memory-cell height up to λm, in order to obtain sufficient cell capacitance, which poses issues of lithography resolution between memory block and peripheral circuits. Conventionally, pre-metal planarization has employed BPSG reflow process, and subsequent low thermal budget and good planarity in STC (stacked capacitor) DRAM devices, and achieved lower leakage current and higher capacitance for Ta2O5 capacitor as well as better planarization performance than those of conventional USG etch back process. No degradation of device characteristics such as Vth change or hot carrier hardness, and gate oxide quality has been observed.

Experimental and Results

FTIR spectra of baked HSQ film at 400°C, thermally annealed HSQ film at 750°C and E-beam cured HSQ film at 400°C are shown in Fig. 1. Both Si-H and Si-O peaks of cage structure disappear after E-beam curing or thermal annealing, which indicates that HSQ film structure becomes similar to that of the conventional oxide film. One of the interesting features is that there are no Si-OH and water peaks after 400°C E-beam curing. Film shrinkage and RI are 23% and 1.48 for thermal curing and 30% and 1.57 for E-beam curing above 6kV, respectively. Therefore, more densified E-beam cured film could prevent water molecules from adsorption. Fig. 2 shows the wet etch rate in 200:1 HF versus the etching depth of E-beam cured HSQ films compared to PE-Ox. Etch rate of E-beam cured HSQ film is ranging from 20 to 30 Å, which is much lower than that of conventional PE-Ox. According to ERD-TOF (Elastic recoil detection-time of flight) data, Si-O ratio of E-beam cured HSQ film at 8keV, thermally annealed HSQ film at 750°C, and PE-Ox are 1:1.4, 1:1.7, and 1:1.8, respectively. It is clear that E-beam cured HSQ film is transformed into Si-rich oxide by E-beam curing. This is the reason why the E-beam cured HSQ film has lower wet etch rate and higher RI value than those of thermally annealed HSQ film and PE-Ox.

Fig. 3 shows the Si 2p spectra of XPS for the differently cured HSQ films.[4] In the high resolution Si 2p spectra, maximum intensity of the E-beam cured HSQ film is 98.1eV, which is lower value than that of thermally cured HSQ film. Also, Si 2p binding from Si-Si bond of E-beam cured HSQ film occurs at 98.1eV, which can not be observed in thermally cured HSQ film at 400°C. These XPS spectra as well as lower Si-O stretching frequency shown in Fig. 1 indicate that the E-beam cured HSQ film has more Si-OH than E-beam annealed. As shown in Fig. 4, the intensity of ESR signal due to the well known generic E defect (single O - vacancy center) having a structure of Si2O5,[5] is much higher in the E-beam cured HSQ films than thermally cured HSQ or conventional oxide films. Fig. 5 is the cross sectional Si-rich oxide damage, which is observed that in the central region, of the boundary region between cell block and peripheral circuits. E-beam cured film shows a smaller porous region than the thermally cured film. It suggests that the E-beam curing provides a much more powerful densification than the thermal annealing even at low temperature.

The influences of E-beam cured HSQ film as PMD on the transistor characteristics are evaluated. Fig. 6(a) is the schematic drawing of the test structure for transistor characterization. Three differently cured HSQ groups and BPSG as a reference were used as PMD. Fig. 6(b) and 6(c) shows Vth distribution and hot-carrier effects of the NMOS transistor with 0.40μm gate length. As clearly shown in Fig. 6, the shift of Vth for the E-beam cured sample is less than 5% compared to the reference samples. Also degradation of hot carrier hardness are not observed. Fig. 7 shows the gate oxide TDBB characteristics for the film area pattern with 150μm x 600μm size during the -10.5V stress condition. There is no deference in the gate oxide quality among E-beam cured HSQ and thermally annealed HSQ samples, which indicate that there are no charge damages from E-beam curing.

The low thermal budget process with HSQ materials using E-beam curing has benefit for the capacitance of dielectric films, especially Ta2O5, for capacitor. As shown in Fig. 8(a), the capacitance for Ta2O5 increases as the thermal budget decreases. The capacitance of the E-beam cured HSQ process at the 5kEV is 7fF/cell higher than that of thermally annealed HSQ process at 750°C. The leakage current level of E-beam cured HSQ process is almost equivalent to thermally annealed sample, as shown in Fig. 8(b).

Conclusion

We developed a new, simple, cost-effective, and very low thermal budget PMD planarization technique of HSQ-coating with E-beam curing. No degradation of transistor characteristics, hot-carrier hardness and gate oxide quality has been observed. This process was successfully applied to STC 256Mb DRAM, in which a superior planarity without film crack was obtained for the high memory cell structure. Also, it was confirmed that high capacitance without increase of the capacitor leakage level can be achieved due to low thermal budget process after Ta2O5 film deposition. We conclude that our planarization technique of HSQ-coating with E-beam curing will be a very promising process for 256Mb DRAM devices and beyond.

References

Fig. 1 FTIR spectra of HSQ with different curing conditions: (a) after 400°C baking, (b) after 750°C annealing and (c) after 400°C E-beam curing at 8 keV and 5000 μC/cm².

Fig. 2 Wet etch rate in 200:1 HF vs etch depth of differently cured HSQ films and PE-oxide.

Fig. 3 High resolution Si 2p spectra of HSQ with curing conditions of thermal baking at 400°C and E-beam curing at 6 or 12 keV, 5000 μC/cm² and 400°C.

Fig. 4 ESR spectra: (a) USG, (b) HSQ/750°C ann. (c) HSQ/6 keV, 5000 μC/cm² and (d) HSQ/12 keV, 5000 μC/cm².

Fig. 5 Incomplete densification of decorated HSQ films at the corner of sidewall in pattern: (a) HSQ/E-beam at 8 keV 5000 μC/cm² and 400°C and (b) HSQ/750°C ann.

Fig. 6 (a) schematic diagram of the test structure for transistor characterization, (b) distribution of Vth for NMOS with gate length of 0.46 μm, and (c) time dependence of hot-carrier degradation with stress condition of Vds=4.5V and Vgs=2.2V.

Fig. 7 Distribution of Ox TDDB at the 150×160 μm² area pattern under -10.5V stress condition for different PMD integration process.

Fig. 8 Capacitor characteristics of TaOₓ for different PMD integration process: (a) distribution of capacitance, and (b) distribution of capacitor leakage.