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Measurement of Copper Drift in Methylsilsesquioxane Dielectric Films

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1. Introduction

Copper (Cu) is a key material for future ultra-large scale integrated circuits (ULSI) because of its low resistivity and high electromigration resistance. Recently, Cu interconnects have been announced as a multilevel interconnect technology for ULSIs [1,2]. Cu interconnects with low-k dielectrics have more advantages to improve high-speed performance of ULSI [3,4]. Thermal diffusion of Cu into SiO_2 interlayer dielectric films is negligible during the fabrication process at temperatures below 450°C. However, the drift of Cu ions (Cu^+ or Cu^{2+}) occurs in the presence of an electric field at temperatures as below as 150°C from the Cu interconnect through SiO_2 to induce leakage currents and degrade devices [5, 6]. In order to understand the mechanism of Cu drift in the dielectric films and to identify Cu barrier requirements for future ULSI integration with low-k dielectrics, the extent of Cu-ion penetration in the dielectric films must be determined [7, 8]. This paper investigate Cu ion drift in methylsilsesquioxane (MSQ) low-k dielectric films using bias-temperature (BT) stress tests and capacitance-voltage (C-V) analysis. The C-V measurement can quantify dielectric charges in metal-insulator-semiconductor (MIS) systems since ionic or dielectric or interface charges affect surface inversion in the semiconductor substrate and thus modify the C-V characteristics such as flat-band shifts.

2. Experiment

In order to investigate Cu drift in MSQ low-k dielectric films, a Al/Cu/MSQ/SiO_2/Si structure was fabricated as shown in Fig. 1. 100 nm thick SiO_2 films were formed by thermal oxidation of n-type Si substrates. Polysilazane precursor solution was spin-coated on the oxidized Si wafers, and baked for 3 minutes at 150-250°C in the air (25°C, 50%RH), then cured for 1 hour at 400°C in nitrogen ambient, so that MSQ films were formed. Table 1 shows the properties of MSQ. Then, a 500 nm thick Cu film was deposited by DC magnetron sputtering on the MSQ film after baked for 30 minutes at 400°C. Then, a 100 nm thick Al film was deposited on the Cu film to prevent the oxidation of the Cu film surface during BT stress. A 500 nm thick Al film was deposited on the backside of the wafer to obtain an ohmic contact. Forming gas (H_2+N_2) anneal was carried out for 10 minutes at 350°C. Cu/Al dots with diameters of 2 mm were patterned by wet etching. The Cu gate electrode serves as a reservoir of Cu ions which can be injected into the underlying dielectric film when an electric field is applied. Al/Cu/MSQ/SiO_2/Si capacitors were biased at elevated temperature ranging from 126 to 165°C to accelerate Cu-ion penetration into the MSQ film. A positive gate bias shifts the C-V curve horizontally in the negative direction. The C-V shifts were quantified by changes in the flatband voltage.

3. Results and Discussion

Figure 2 shows C-V characteristics of an Al/Cu/MSQ/SiO_2/Si-substrate capacitor measured at room temperature, which was biased at 20V at 165°C for 2, 4 and 6 minutes, respectively. The amount of Cu^+ charge drifted into the stacked MSQ and SiO_2 films can be estimated from the measured flatband voltage, V_{FB}. V_{FB} can be expressed as follows.

$$V_{FB} = -\int_0^{d_1+d_2} \omega(x)\rho(x)dx \qquad (1)$$

where, d_1 and d_2 are thicknesses of MSQ and SiO_2, respectively. $\omega(x)=x/\varepsilon_{MSQ}$ $(0\le x\le d_1)$, $\omega(x)= d_1/\varepsilon_{MSQ} + (x-d_1)/\varepsilon_{SiO2}$ $(d_1\le x\le d_1+d_2)$. $\rho(x)$ is a Cu ion distribution in the film. Assuming the Cu ions had drifted and accumulated at the SiO_2/Si interface, the Cu^+ concentration per unit area, $[Cu^+]$ is

$$[Cu^+]=-C_{ILD}\bullet\Delta V_{FB}/q \qquad (2)$$

where C_{ILD} is the series stacked capacitance of SiO_2 and MSQ per unit area, ΔV_{FB} is a flatband voltage shift and q is the electronic charge. As BT stress time increases ΔV_{FB} becomes more negative, indicating more positive charge is introduced into the dielectric film. Dependence of BT voltage and temperature on ΔV_{FB} are shown in Fig. 3 and Fig. 4, respectively. ΔV_{FB} increased with increasing applied voltages and stress temperatures. The Cu^+ drift rate in the MSQ dielectric film was calculated by eq. (2), and it was between the reported values in PECVD-SiO2 and PECVD-oxynitride [7].

4. Conclusion

Measurement of Cu drift in MSQ low-k dielectric films in the presence of an electric field was conducted using bias-temperature stress tests and capacitance-voltage analysis. It is found that Cu ions drift with stress time, voltage, and temperature. The Cu^+ drift rate in a MSQ dielectric film was between the reported values in PECVD-SiO2 and PECVD-SiON.

Acknowledgement

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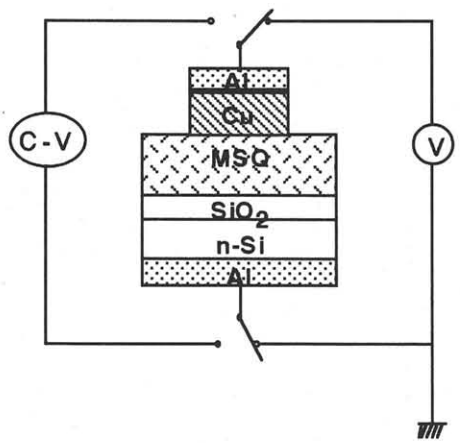

Fig.1. Sample capacitor structure and measurement setup. Al(100nm)/Cu (500nm)/MSQ(4000nm)/SiO_2(100nm)/Si.

Table 1 Properties of MSQ

Structure	$(CH_3)SiO_{1.5}$
Dielectric Constant	2.5
Refractive Index	1.45
Density	1.2
Film Stress	$1.0x10^9$ [dyn/cm^2]

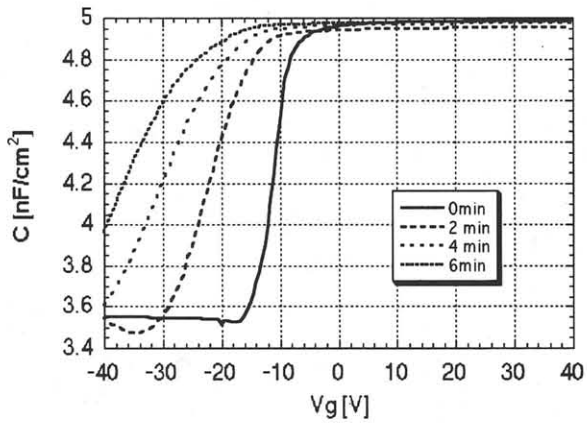

Fig. 2. C-V curves of MSQ capacitors stacked with SiO_2 as a parameter of BTstress time. BT stress condition is +20V Cu gate bias at 165°C in N_2.

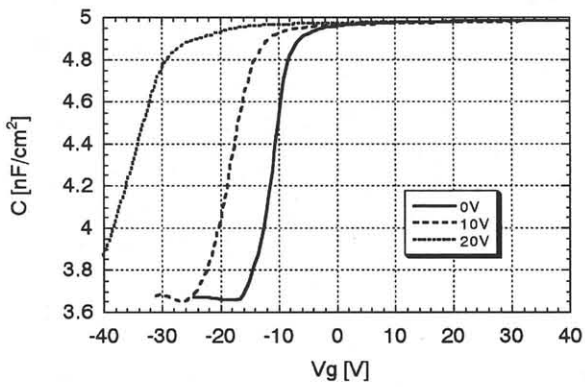

Fig. 3. C-V curves of MSQ capacitors stacked with SiO_2 as a parameter of bias voltage. BT stress time is 10 minutes at 165°C in N_2.

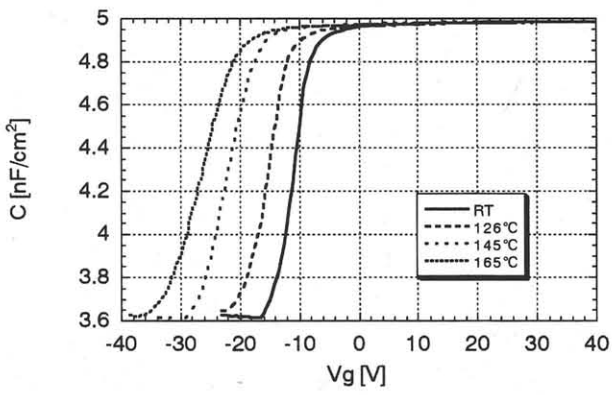

Fig. 4. C-V curves of MSQ capacitors stacked with SiO_2 as a parameter of temperature. BT stress condition is 20V for 10 minutes.