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Improvement in Sheet Resistance of Sb-Doped Ultra Shallow Junction by Dopant Pileup Reduction at the SiO_2/Si Interface

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1. Introduction

Reduction of parasitic resisrtance is becoming more important as the MOSFETs gate length is scaled and channel resitance is reducecd. From this viewpoint, sheet resiatance of source and drain junctions should not be increased by the scaling of junction depth which is necessary for short channel effect suppresion. We have demonstrated ultra shallow(19 nm) and low resitive(1.4 kΩ/sq.) n^+/p junction formation by 10 keV Sb implantation and its application to 0.15 μm MOSFETs [1]. Formation of shallower junction is not so difficult by reducing the implantation energy because of low diffusive nature of Sb. However, improvement in sheet resistance(R_s) is more important than the shallower junction for the further scaling. We have reported that dopant loss due to the pileup of Sb at the SiO_2/Si interface is an obstacle for the R_s improvement [1,2]. We have for the first time confirmed that an RTA(Rapid Thermal Annealing) method is effective for the redcution of pileup and the improvement in R_s and report in this paper.

2. Experimental

Antimony ions were implanted into p-type Si(100) substrates with a 5 nm screen oxide at a dose of $1x10^{13}$-$3x10^{14}$ cm^{-2}. Implantation energy was10 KeV for all cases. Furnace annealing(FA) or RTA were performed in N_2 for the dopant activation. In the case of RTA, the screen oxide was not removed to prevent out diffusion during the annealing. In the case of FA, the screen oxide was removed prior to the annealing and typically 2-nm-thick oxide grew on Si during the annealing. Arsenic implantation and annealing were also carried out in the same manner for comparison.

Sheet resitance of the implanted layer was mainly evaluated by the four point probe method. Hall measurements for some specimens proved the accuracy of results of the four point probe method. Antimony depth profiles were evaluated by SIMS measuremants. Stripping of surface SiO_2 film on Si prior to the SIMS mesurements was not carried out with a few exception, since the pileup is also removed by HF treatment for the stripping [1,2]. Junction depth was estimated from the depth profiles assuming the substrate acceptor concentration to be $5x10^{17}$ cm^{-3}.

3. Results and Discussion

Figure 1 shows depth profiles of Sb obtained for several implantation doses. Furnace annealing temperature and time were 850 °C and 30 min, respectively. This figure indicates that the amount of pileup and dopant loss increases as the Sb dose incrases. Therefore, effective reduction in R_s by increasing the implantation dose is difficult without pileup reduction. The dopant loss due to the pileup amounts to 60% for the implantation dose of $1x10^{14}$ cm^{-3} [2]. By FA at lower temperature of 700°C the pileup became much smaller compared with the 850°C case. Sheet resistance was improved to 1.0 kΩ/sq. as shown in Table 1. However, estimated activation rate of Sb was about 55% which is probably due to too low annealing temperature. Shortening of annealing time by RTA was also effective to reduce pileup as shown in Fig. 3. For the 800°C and 900°C RTA, Rs was improved to 0.84 kΩ/sq. as shown in Table 1. The improvement is a result of reduction in the dopant loss due to the pileup reduction and high activation rate larger than 80% for highly doped region shown in Fig. 4. In the case of 1000°C RTA in Fig. 3, the pileup and larger diffusion are observed. The mechanism of pileup is not clearly explained up to now. We qualitatively explained it that the SiO_2/Si interface works a "sink" for dopants and some transient mechanisms to transport dopants to the Si surface exist [2]. The similar pileup of As has been also reported, however, its behavior has been investigated for limited implantation and annealing condition [3-5]. Figure 5 shows depth profiles of As. At the same condition as Fig.3, As showed the clear pileup and the sheet resistances were about 1.1 to 1.2 kΩ/sq. which are higher than those for Sb.

The Relationships between the junction depth X_j and R_s are summarized in Fig. 6. By utilizing the RTA technique, R_s was reduced to 0.84 kΩ/sq. keeping X_j to be 19 nm. Furthermore, by Increasing the dose to $3x10^{14}$ cm^{-2} R_s was improved to 0.45 kΩ/sq. for 800 °C RTA. Junction depth was about 24 nm and Increase was only about 5 nm. Since X_j for As shown in Fig. 5 was about 30 nm, these results are evidences of good suitability of Sb for ultra shallow and low resistive junction formation for sub-0.1-μm MOSFETs.

4. Conclusions

We have for the first time found that the Sb pileup can be reduced by the RTA technique. As a result, R_s of 19-nm-deep junctions were decreased down to 0.84 kΩ/sq. By increasing the implantation dose, 24 nm X_j and 0.45 kΩ/sq. R_s were also obtainable. These results will support performance improvement of MOSFETs to sub-0.1-μm generations.

Acknowledgments

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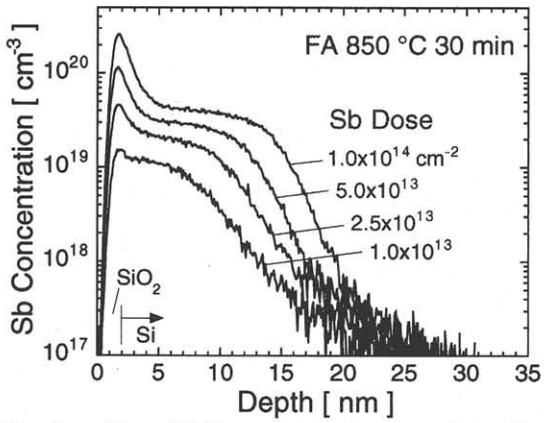


Fig. 1 Depth profiles of Sb for various implantation doses. FA stands for furnace annealing. The pileup becomes more conspicuous as Sb implantation dose increases.

Table I Sheet Resistance of n^+ Implanted Layers

	Annealing Condition	Sheet Resistance Rs [kΩ/sq.] Sb $1x10^{14}$ cm^{-2}	Sb $3x10^{14}$ cm^{-2}	As $1x10^{14}$ cm^{-2}
FA	850 °C, 30 min	1.4		1.7
	700 °C, 60 min	1.0		
RTA	800 °C, 10 s	0.84	0.45	1.1
	900 °C, 10 s	0.84	0.55	1.1
	1000 °C, 10 s	1.0		1.2

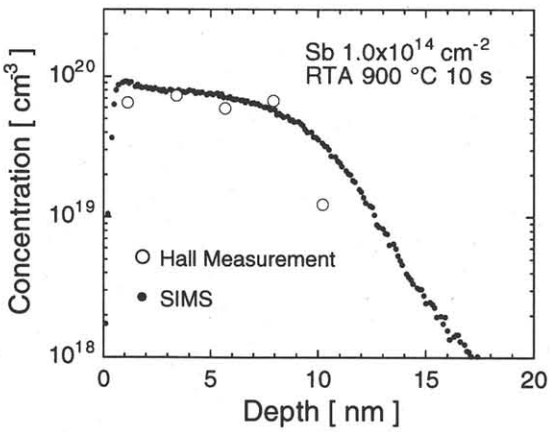
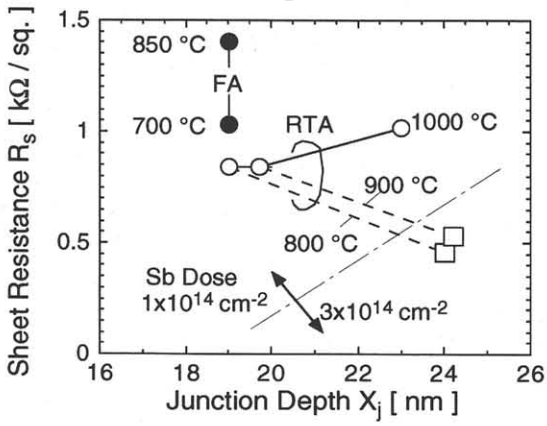


Fig. 4 Comparison of a carrier depth profile obtained by differential Hall measurement (open circles) and a Sb SIMS depth profile (dots). Prior to these measurements, SiO_2 on Si was removed.



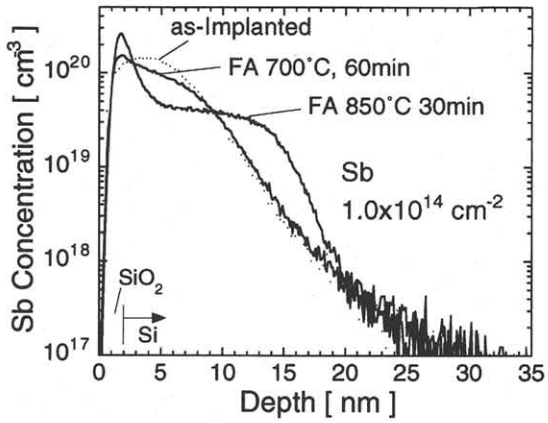


Fig. 2 Influence of furnace annealing temperature on Sb depth profiles. The pileup is reduced by lowering the annealing temperature down to 700°C.

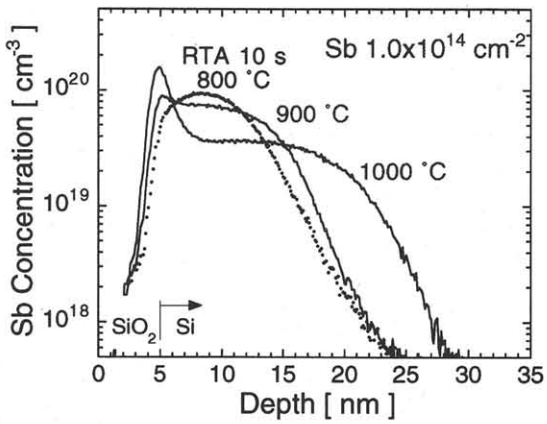


Fig. 3 Influence of RTA (Rapid Thermal Annealing) temperature on Sb depth profiles. The pileup is not conspicuous for the 800°C and 900°C cases. On the contrary, RTA at 1000°C gives rise to the clear pileup like FA at 850°C in Figs. 1 and 2.

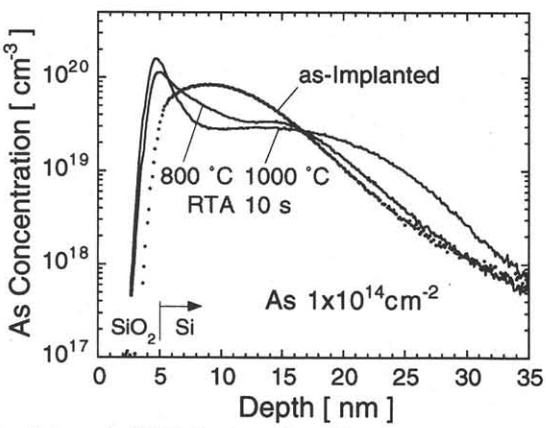


Fig. 5 Arsenic SIMS depth profiles. The pileup cannot be reduced by RTA unlike the Sb cases in Fig. 3.

Fig. 6 Relationship between sheet resistance and junction depth. Sheet resistance is decreased by RTA at 800°C or 900°C. This decrease is attributed to the pileup reduction shown in Fig. 3. Sheet resistance can be reduced down to 500 Ω/sq. by increasing Sb implantation dose to $3x10^{14}$ cm^{-2}. The junctions are shallower than 25 nm for all cases and are shallow enough for sub-0.1-μm MOSFETs.