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# Dopant-Induced Defects Formed by Ion Implantation -Dopant Species Dependence-

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## 1. Introduction

In order to realize future high-performance LSIs, total low-temperature processing, which suppresses dopant redistribution and allows us to employ new materials, is essential. However drastic increase of junction leakage current caused by residual defects, with the decrease of the temperature of the post implantation annealing, has been one of the most crucial problems for establishing total low-temperature processing. In our previous research, by eliminating possible contamination [1], and by using low dopant concentration substrate [2,3], it has been achieved very low leakage current (~1nA/cm$^2$) $n^+p$ and $p^+n$ junctions annealed at as low as 450°C [3] (**Fig. 1**). It is very surprising that the leakage current is exponentially decreased with the decrease of the substrate dopant concentration. This result implies that the dopants could act as defects (carrier generation center). In other experiments, it has been confirmed that these defects causing the leakage current are distributed much deeper in the substrate than the implanted region [2]. From above experimental results, we have suggested the model of this "dapant-induced defect" formation as follows; the point defects (interstitial/vacancy) generated in the ion-implanted region diffuse into the substrate and then they are captured by the dopants in lattice-site (**Fig. 2**). "Ultra-cleanest ion implantation" would not able to suppress the generation of the "dopant-induced defect". We believe this defect is the "final" defect that must be overcome.

In this paper, the characteristics of this "dopant-induced defect" are studied with the consideration of dopant species by the measurement of bulk generation lifetime ($\tau_g$) and its temperature dependence. Also, $\tau_g$ dependence on the annealing temperature has revealed the thermal stability of this defect.

## 2. Experimental

The special samples named "damaged MOS capacitor" were prepared. The MOS capacitors (phosphorus-doped and boron-doped) having various substrate dopant concentration ($N_{sub}$) were damaged by $Si^+$ ion implantation (50 keV, $1x10^{12}cm^{-2}$) after gate oxide formation, in order to form the "dopant-induced defect" in the substrate. Then the samples were annealed at 450-1000°C for 5 hours or 1 hour in $N_2$ (**Fig. 3**). After Aluminum gate electrode formation, forming gas treatment was carried out.

## 3. Results and Discussion

In **Fig. 4**, the bulk generation lifetime ($\tau_g$) of "damaged MOS capacitor" is plotted as a function of substrate dopant concentration ($N_{sub}$). $\tau_g$ was obtained from the Zerbst plot of pulsed MOS C-t response [4]. The figure clearly shows that $\tau_g$ decreases exponentially with the increase of $N_{sub}$, for both phosphorus-doped and boron-doped. This tendency agrees with the result of **Fig. 1**. Surprisingly $\tau_g$ of boron-doped is smaller than that of phosphorus-doped by more than one order of magnitude.

**Figure 5** shows the temperature dependence of $\tau_g$. It can be seen that there is no temperature dependence of $\tau_g$ for both phosphorus-doped and boron-doped. Since $\tau_g$ is given by

$$\tau_g = (\sigma v_{th} N_t)^{-1} \exp(|E_t - E_i|/kT) \quad (1)$$

from SHR model ($\sigma$: capture cross section, $v_{th}$: carrier thermal velocity, $N_t$: trap density, $E_t$: trap energy level, $E_i$: intrinsic Fermi level), this result indicates that $E_t$ is located at $E_i$, and $\tau_g$ becomes

$$\tau_g = (\sigma v_{th} N_t)^{-1}. \quad (2)$$

Assuming $\sigma$ of phosphorus-doped and boron-doped are the same, it could be said that $N_t$ of boron-doped is about one order of magnitude larger than that of phosphorus-doped, from the result of **Fig. 4**. This result implies that boron in lattice-site captures point defect more easily than phosphorus does. We believe this is due to the difference of the local stress which is caused by the difference of the atomic radius of silicon and the dopant.

In **Fig. 6**, the dependence of $\tau_g$ on the annealing temperature is shown. It can be seen that $\tau_g$ is recovered, which means the defect is annealed-out, at about 800°C for both phosphorus-doped and boron-doped. This temperature of 800°C is not acceptable for establishing total low temperature processing. Therefore, the generation of the "dopant-induced defect" must be suppressed. So far the use of low dopant concentration substrate will be the only answer.

## 4. Conclusion

We have shown that the "dopant-induced defect" is formed more easily in boron-doped silicon than phosphorus-doped silicon by ion implantation. The defect forms the trap energy level at intrinsic Fermi level in the band gap of silicon. The defects are annealed-out at about 800°C. In order to achieve very low leakage current junctions even by low-temperature annealing, it is essential to use as low dopant concentration substrate as possible, in addition to ultra-clean

ion implantation [1]. This technology is applicable to the formation of source/drain of MOSFET on an intrinsic SOI layer.


## Acknowledgment

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## Reference


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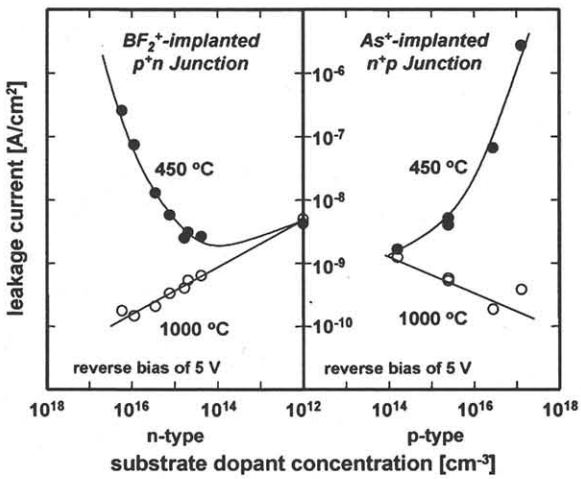


**Fig. 1** Leakage current density at reverse bias of 5V plotted as a function of substrate concentration ($N_{sub}$) for both $As^+$-implanted $n^+p$ junction and $BF_2^+$-implanted $p^+n$ junction annealed at 450°C and 1000°C.

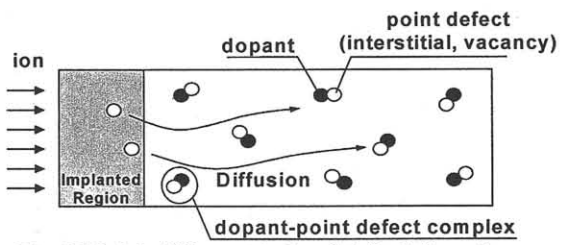


**Fig. 2** Model of "dopant-induced defect" formation.

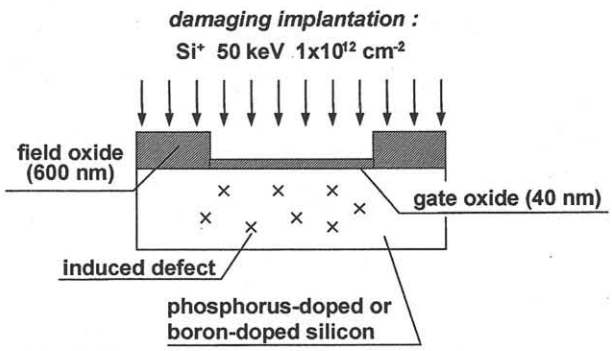


**Fig. 3** Schematic picture of special sample named "damaged MOS capacitor".

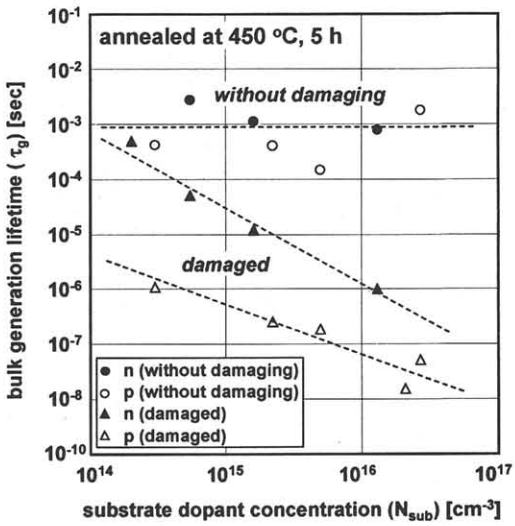


**Fig. 4** Bulk generation lifetime ($\tau_g$) of "damaged MOS capacitor" plotted as a function of substrate dopant concentration.

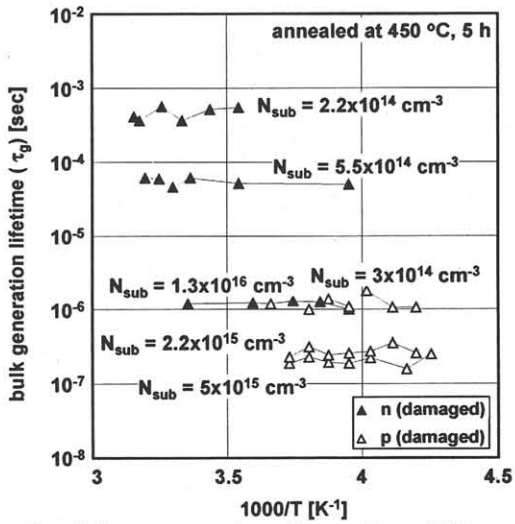


**Fig. 5** Temperature dependence of $\tau_g$ of "damaged MOS capacitor".

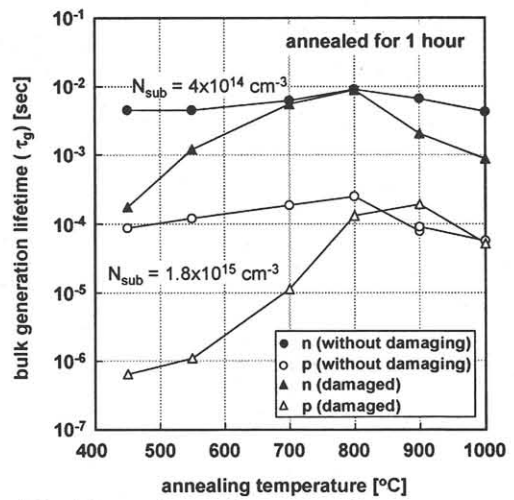


**Fig. 6** Dependence of $\tau_g$ on annealing temperature.