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High Performance Buried Channel-pFETs Using Elevated Source/Drain Structure with Self-Aligned Epitaxial Silicon Sliver (SESS)

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1. Introduction

Elevated source/drain (ESD) made by selective epitaxial growth (SEG) displays distinctive facets [1] near the gate sidewall spacers. This faceting causes a slight degradation of DIBL [2] due to the locally deeper junction beneath the epi-facets. Various innovative techniques [2,3] including 2nd spacers to cover the facets have been proposed, but they give rise to another process complexities.

In this paper, we present that ESD formed without any additional process reveals the excellent short channel characteristics by employing the self-aligned epitaxial silicon sliver (SESS). By employing a dual spacer structure of HTO and nitride, the SESS protruding laterally into the bottom edge of gate sidewall spacers was intentionally formed to increase the surface counter-doped boron concentration of BC-pFET while minimizing the faceting. Trade-off between SESS and facet development is also revealed by the control of HTO thickness. As a result, the increased drain current without short channel degradation was obtained using ESD with SESS. At the same time, we also report that SESS induced spacer undercut [4] leads to the negative slope of sidewall spacers, and in turn minimizes the faceting with a help of stacking faults (SF) [5].

2. Experimental

After shallow trench isolation formation, BC-pFETs with standard triple well CMOS process were fabricated. V_t was adjusted by BF_2/3.2E12/25keV implant through 50Å thick screen oxide. After 65Å thick gate oxidation, 1500Å thick WSi_x/Poly-Si gate with 1800Å thick mask oxide were formed. For intentional introduction of SESS while making ESD, double spacer structure such as 100Å HTO/700Å nitride was adopted, as shown in Fig.1. Then, SEG was carried out using $SiH_2Cl_2/HCl/H_2$ source gases at 850°C for 3 min along with in-situ H_2 pre-bake at 900°C for 1 min. After source/drain implantation, RTA at 950°C for 20 sec was done to activate the dopants. To fabricate the test pattern, 2.5μm deep and 0.35μm wide contact holes were etched. Sputtered 500Å thick Ti and 600Å thick TiN were sequentially deposited onto the contact hole with a good step coverage.

3. Trade-off between facets and SESS developments

Control of HTO thickness provides a trade-off between facet minimization and overall length of SESS, as shown in Fig.2. The SFs developed severely with increasing undercut feature mitigates the intrinsic faceting which is determined thermodynamically, and results in the suppressed facet near gate spacers. Overall morphology of SESS including some amounts of SF is rather good and the interface between SESS and substrate disappears, as shown in Fig.3. Therefore, more efficient B supply into the channel region is possible without any segregation due to the interface during annealing.

4. Short Channel Characteristics

Fig.4 shows the measured and simulated linear V_t behavior with mask channel length. Simulated V_t's are based on 2-D doping profiles where the steep profile of locally deeper junction edges beneath the epi-facets is relaxed due to facet suppression by SESS, as shown in Fig.5, and are in good agreement with measured data. Compared to the BC-pFETs using non-elevated conventional junction (NECJ) implanted at BF_2/3E15/12keV, remarkably improved roll-off characteristics were obtained at BF_2/3E15/30keV implant condition. Increasing BF_2 dose to 7E15 could decrease V_t of ~75mV due to deeper junction while maintaining the good roll-off behavior. DIBL results obtained at 3E15 dose were improved, as shown in Fig.6, without degrading saturation drain current (IDSAT). Improved IDSAT characteristics are due to SESS acted as a boron provider to increase the surface counter-doping concentration of BC-pFET. Fig.7 shows the simulated IDSAT profiles of SESS and conventional (non-sliver) ESDs. As closer to short channel regime, the increase of IDSAT became remarkable in BC-pFET ESD employing SESS due to sliver induced higher B concentration, compared to conventional ESD. Under the high dose of 7E15, the increase of IDSAT became more eminent due to both the lowered V_t and increased SESS effects. In spite of the lower V_t due to deeper junction, the short channel degradation in case of 7E15 was not so severe compared to the result of NECJ. Along with DIBL, the channel punchthrough and S-factor were remarkably improved, as shown in Fig.8. In spite of the shorter distance between ESD and gate oxide due to SESS (see Fig.3), TDDB characteristics under constant-current stress was not degraded as shown in Fig.9.

5. Junction Leakage and Contact Characteristics

Cumulative characteristics of p^+/n well junction leakage at 5V reverse bias are rather improved in spite of severe SF formations, compared to NECJ as shown in Fig.10. In addition, contact resistance and its uniformity are also improved due to highly B doped SEG grown contact pad, as shown in Fig.11. Especially, the chain resistance of serially connected contacts is about ten times lower than one of NECJ.

6. Conclusions

High performance BC-pFETs employing ESD with SESS were obtained for extending the application below sub-0.25μm range. Remarkable improvement of V_t roll-off, DIBL, BVDSS and other short channel characteristics was presented without the degradation of GOI. Increased IDSAT due to SESS as a B provider was then obtained.

References

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[2] J. J. Sun et al., IEEE ED-45 [6], p1377 (1998)
[3] C. -P. Chao, et al., IEDM, p103 (1997)
[4] K. Miyano et al., Ext. Abst. of SSDM, p420 (1998)
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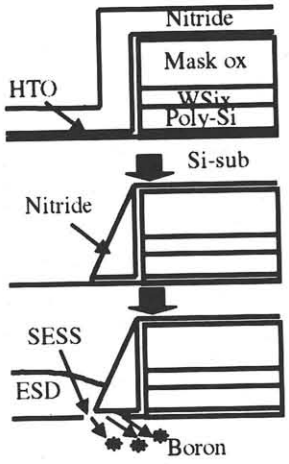


Fig.1 Fabrication flow of ESD employing SESS.

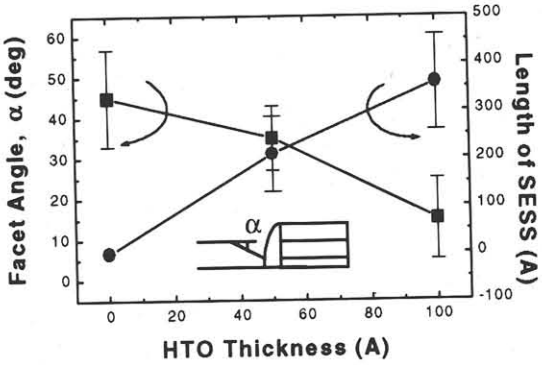


Fig.2 Trade-off relation between facet angle and length of SESS. Facet angle (α) is controlled by the amount of stacking faults developed on the edge of SEG mesa close to nitride spacers [5].

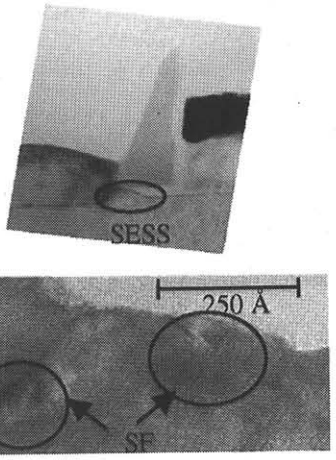


Fig.3 XTEM micrograph showing SESS with some SF. Bottom photograph is the HREM image of SESS.

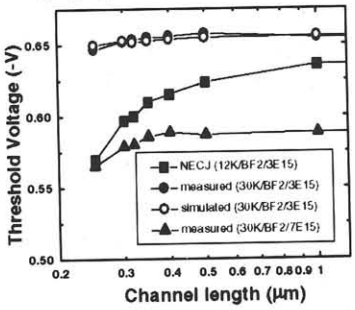


Fig.4 Measured and simulated V_t profiles with mask channel length.

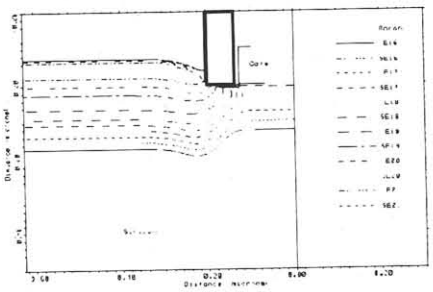


Fig.5 2-D doping profile. Facets suppressed by SESS minimize the steep profile of locally deeper junction edges beneath the epi-facets.

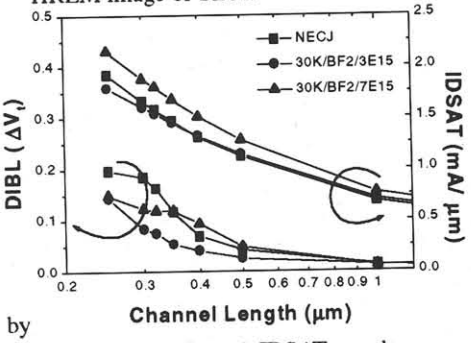


Fig.6 DIBL and IDSAT results as a function of channel length.

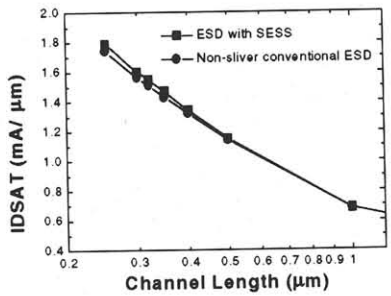


Fig.7 Simulated IDSAT results of SESS and non-sliver ESDs as a function of channel length.

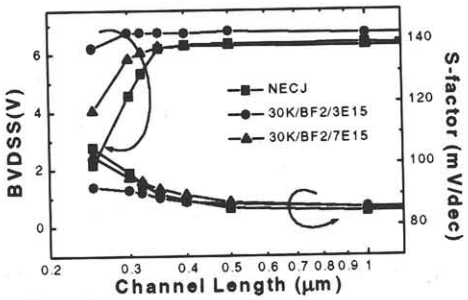


Fig.8 Channel punchthrough and S-factor with channel length. ESD with SESS reveals the remarkably improved performances, compared to NECJ.

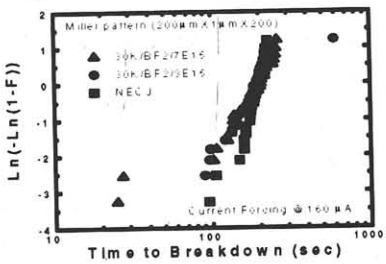


Fig.9 TDDB characteristic under constant-current stress is not degraded in spite of SESS application.

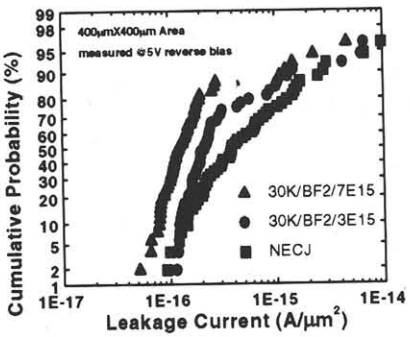
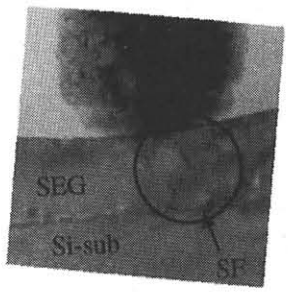


Fig.10 Cumulative characteristics of Junction leakage are improved by ESD application with SESS.



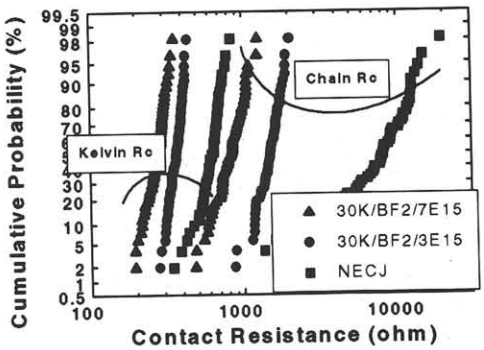


Fig.11 Cumulative characteristics of Kelvin- and chain (10K array)- contact resistance are shown along with XTEM micrograph showing the contact region.